PHOENIX-D48 CPCI CAMERA LINK

CONDUCTION COOLED DIGITAL FRAME GRABBER

- Single Base, Dual Base or Medium Camera Link Configurations.
- 3U CompactPCI form factor.
- Optional conduction cooled assembly.
- 32 bit 66MHz PCI support in 3.3V signalling environments.
- Maximum PCI burst rate of 266Mbytes/sec.
- Supports digital areascan / linescan cameras.
- Accepts multi-tap & multi-channel camera formats, including line and pixel interleaved.
- -40°C to +85°C extended temperature operation.
- Software Development Kit (SDK) supports various operating systems for rapid integration.
- v2.2 PCI and v1.2 Camera Link compliant.
- Support for PoCL including *SafePower*.
- Bus mastering hardware control of scatter-gather requires 0% host CPU intervention.
- Supports Camera Link serial comms API.
- Implements Data Valid (DVAL) for slow data rate cameras.
- Opto-Isolated, TTL and EIA-644 I/O.
- Utilises software configurable FPGA technology for maximum flexibility.
- Optional rear panel I/O adapter available.
- RoHS compliant.

Active Silicon
COMPUTER IMAGING PRODUCTS

OVERVIEW

Phoenix-D48CL is a CompactPCI board for the acquisition of digital data from a variety of Camera Link sources, including digital frame capture and line scan cameras. It supports all the formats of the Base and Medium configurations, i.e. single 8 to 16 bit data, through 12 bit RGB, to four tap 12 bit sources, as well as dual Base configuration, i.e. acquisition from two asynchronous Base cameras.

Phoenix-D48CL also supports various camera tap formats, such as line interlaced - adjacent lines are output simultaneously; line offset - lines are output from different parts of the CCD simultaneously; pixel interlaced - adjacent pixels on the same line are output simultaneously; and pixel offset - pixels are output from different parts of the same line simultaneously.

Phoenix-D48CL supports the Power over Camera Link (PoCL) functionality with *SafePower* and is able to provide power to PoCL enabled cameras via the Camera Link data cable thereby removing the need for a separate power supply. Conventional non-PoCL cameras are still supported.

ROI and sub-sampling controls are used to increase application processing speed by only storing the required data. In addition the LUT functionality provides support for gamma correction, dynamic range cropping and binary thresholding in real time. The DataMapper further reduces the load on the host processor by mapping and packing the acquired data prior to transfer across the PCI bus. For example, the acquired data can be mapped into a suitable format and transferred directly to the graphics display, without the need for any host processing.

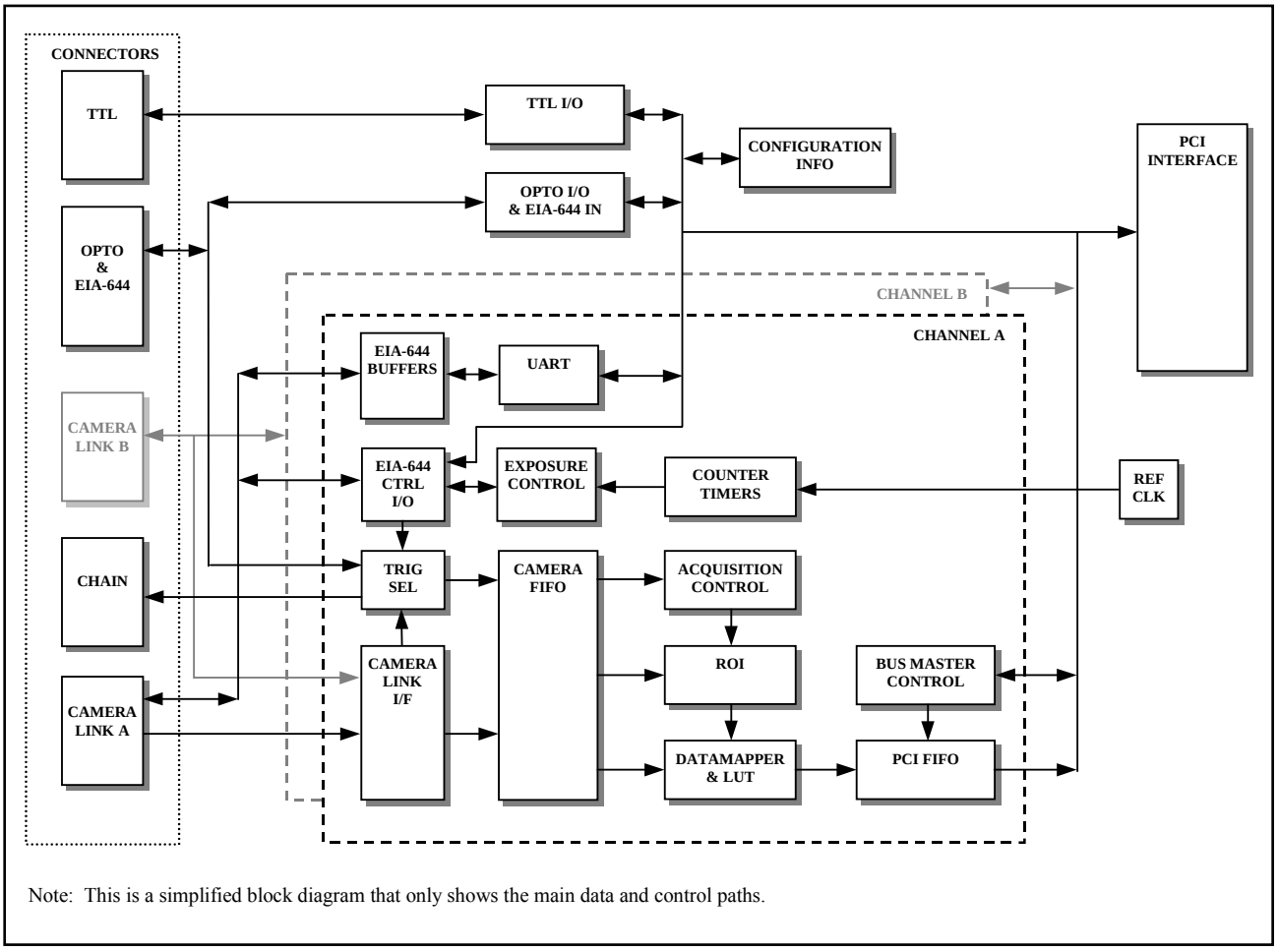
The PCI interface comprises intelligent scatter-gather hardware which reads its instructions direct from memory without any host CPU intervention. This in turn controls the DMA engine, which transfers the packed video data into any target memory which can be reached from the PCI bus. This can be system memory, graphics memory, or even other devices on the same or other PCI busses, such as DSP cards, etc.

The majority of the functionality is implemented in a single FPGA (Field Programmable Gate Array) providing a flexible solution for interfacing to Camera Link compliant sources. The FPGA implements the PCI interface, hardware

scatter-gather control, PCI Initiator Burst Control (DMA), Acquisition Control, Region of Interest (ROI) and sub-sampling control, DataMapping functions, Datapath FIFOs, and Counter/Timer support. In addition the board contains Look Up Table (LUT) functionality, a dual Universal Asynchronous Receiver Transmitter (UART), 4 bit opto-isolated I/O, two 2 bit differential input ports and two 8 bit TTL I/O ports. All I/O is accessible on the J2 connector.

The Software Development Kit (SDK), available as a separate item, allows rapid system development and integration. It provides comprehensive example applications and optimized libraries, and is available for a variety of operating systems via a common API, including Windows and Linux (32 bit and 64 bit environments) as well as Mac OS X, DOS, VxWorks and QNX. Drivers for third party applications are also available, Common Vision Blox, Image-Pro Plus, StreamPix, Labview etc. As well as functions that control the hardware, the libraries include general purpose functions for the manipulation and display of images. A separate datasheet describes the SDK in detail.

SYSTEM BLOCK DIAGRAM



Note: This is a simplified block diagram that only shows the main data and control paths.

HARDWARE SPECIFICATION

Camera Clock:	***Phoenix*** supports effective clock rates from DC to 60MHz, using the Camera Link Strobe (STB) and Data Valid (DVAL) signals. For faster speeds contact your distributor.
Camera FIFO:	Data from the video source is stored in a FIFO prior to being processed by ***Phoenix***. For certain high bandwidth applications it is possible to extend the FIFO size - please contact your distributor for more details.
Acquisition Control:	The acquisition trigger control module is used to determine which video frames to acquire from the camera. The system can be configured for a single trigger event to acquire all subsequent frames, a trigger event per frame, or continuous acquisition irrespective of the trigger condition. The trigger event is programmable between level or edge sensing on one of the opto-isolated or EIA-644 control inputs. When running in linescan mode, there is an additional mode that uses the active trigger input as an envelope signal. In this mode all lines are acquired whilst the trigger input is asserted. The hardware can also delay the trigger event by a fixed time period or number of lines, and allows the trigger event transducer to be located remotely from the camera.
Region of Interest:	The Region Of Interest (ROI) controls which part of the camera output data to acquire. In areascan mode, this is a rectangular region with software programmable width, height and x / y offset. Linescan mode is similar, allowing control of the width and x offset, with the height control being used to package the data into pseudo frames for subsequent processing by the user's application. ***Phoenix*** supports an additional mode (DataStream) whereby data is acquired based upon the control inputs, e.g. all data is acquired when Frame Valid (FVAL) and Line Valid (LVAL) are both asserted. This is necessary for cameras that output their own arbitrary ROIs within a single video frame, or those that vary the amount of data output on each line.
Sub-Sampling:	Software controlled hardware sub-sampling is also supported. A factor of x1, x2, x4 or x8 can be independently selected for both x and y directions, e.g. a horizontal factor of x4 and a vertical factor of x2 would acquire every 4th pixel across a line and every 2nd line down the frame.
DataMapper:	The raw camera data can be reformatted in hardware for ease of subsequent processing. For example, a mono data source can be converted into 32 bit color data, ready to be sent directly to graphics card memory, thus reducing the host processor overhead. The optimum use of system resources is determined by the user's application, e.g. packing mono data into 32 bit color reduces the host processor overhead at the expense of increasing the amount of data transferred across the PCI bus. The output formats supported include, 8, 16 and 32 bit mono, as well as 15, 16, 24, 32 and 48 bit color in both RGB and BGR ordering, thus supporting big and little endian processor formats.
LUT:	A 16 bit in, 16 bit out (i.e. 65,536 by 16) LUT per channel allows arbitrary mappings between the input data from the video source and the output data to the destination memory. This allows functions such as gamma correction, brightness, contrast and thresholding to be performed in real time in hardware on a per color or per camera basis. The LUT may also be used to shift the LSB aligned video data to MSB alignment ready for processing.
PCI FIFO:	A 1024 by 64 bit FIFO per channel provides buffering between the camera and the PCI bus. If the board is being used in single camera mode, then both channels are used providing a 2048 by 64 FIFO.

Bus Master Control:	Core to ***Phoenix*** is a dedicated RISC processor and a highly optimised PCI Bus Master (DMA) engine. The RISC processor reads transfer length and destination address instructions across the PCI bus from host memory, and loads these into the PCI Bus Master engine with no host CPU overhead. The DMA engine then transfers the video data at the full PCI bus rate into host memory, thus achieving the maximum burst rate of 266MBytes/sec. When the current instruction has completed, the RISC processor optionally generates a PCI interrupt to signal that the transfer has completed, before either halting or retrieving the next instruction. The RISC processor also supports jump instructions that allow a single piece of RISC code to continuously loop without any CPU intervention.
Interrupts:	An interrupt signal is available, and can be configured via software to interrupt on a number of different events, including acquisition complete, FIFO overflow, Start/End of Frame/Line, etc.
Counter Timers:	Four 32 bit counter timers are available for each channel of the ***Phoenix***. The counter timers are dedicated for the following functions: 1. Astable timer used as a line rate generator for linescan cameras, or as an acquisition trigger for areascan cameras, thus controlling the overall frame rate. The period of the astable can be set from 1µs up to 70 minutes in 1µs increments. 2. Dual monostables for generating two exposure output signals, e.g. ExSync and PRIN. Both monostables are triggered by the same software selectable event but can be programmed with different time periods, once again to 1µs resolution. This provides a flexible exposure control system. 3. Trigger delay counter used to postpone acquisition triggering by a programmable time delay or line count. This allows the acquisition trigger sensor to be mounted remotely from the camera. (Note: As the counter is non-retriggerable, subsequent trigger events will be ignored until a pending event has completed its delay). 4. A versatile event counter is provided to count a number of different events types - Lines (LVAL), Frames (FVAL) or microseconds, within a specified gate condition - Line (LVAL), Frame (FVAL), Acquisition Trigger or Entire Acquisition. The event count provides readings for both the current value, as well as the final value at the end of the previous gate condition. For example the event counter can be configured to provide the current line number within a frame, as well as the total number of lines in the previous frame. Other uses include providing the frame period, the number of lines in the previous acquisition trigger envelope – and hence how much data there is to process, or the number of images processed so far.
Camera Control Outputs:	Two 4 bit EIA-644 (LVDS) output ports are provided to interface with the camera. Each bit can be individually set to a logical “1” or “0” under software control or used to drive the camera with exposure control pulses from the counter timer module. The ports are on the Camera Link interface on the CompactPCI J2 connector and the rear panel I/O adapter. See the *Connector Pinouts* section for more details.
Opto-Isolated I/O:	4 bits of opto-isolated I/O are provided to interface to external systems. As standard, ***Phoenix*** is configured with 2 bits of input and 2 bits of output, but this can be varied as factory build option - please contact your distributor for further information. The outputs are designed to sink up to 20mA, and will withstand 24V when “off”. The inputs sense voltages between 3.3V and 24V as a logic high input. A 4.7kΩ current limiting series resistor is fitted on all inputs. The outputs can be individually set and cleared via software, controlled from the internal timer resources, or fed from other input events, e.g. acquisition triggers, etc. The Opto-Isolated I/O signals are available on the CompactPCI J2 connector and the rear panel I/O adapter. See the *Connector Pinouts* section for more details.

EIA-644 Control In:	Two 2 bit EIA-644 (LVDS) input ports are provided to interface with other systems. They can be used to read status information from the camera, as additional acquisition trigger sources, or as inputs from shaft encoders, etc. The LVDS I/O signals are available on the CompactPCI J2 connector and the rear panel I/O adapter. See the *Connector Pinouts* section for more details.
TTL I/O:	Two 8 bit TTL I/O ports are provided to interface with other systems. Each 8 bit port can be independently configured as all input or all output under software control. When used as outputs, each bit can source 24mA at min 2.2V or sink 24mA at max 0.55V. When used as inputs, an applied voltage of between 2V and 5V is read as a logical "1" and an applied voltage of between 0V and 0.8V as a logical "0". The TTL I/O signals are available on the CompactPCI J2 connector. See the *Connector Pinouts* section for more details.
Serial Port:	***Phoenix*** is fitted with a dual channel Universal Asynchronous Receiver Transmitter (UART), containing 64 character hardware transmit and receive FIFOs for each channel (the software libraries buffer the transmit and receive data to provide larger user FIFOs). Each channel independently supports 1, 1.5 or 2 stop bits; 5, 6, 7 or 8 data bits; and odd, even or no parity. The baudrate can be configured with standard values from 300 baud up to 115,200 baud. ***Phoenix*** also supports software (XON, XOFF) flow control within the UART without host CPU intervention.
Connectors:	***Phoenix*** is fitted with the both J1 and J2 CompactPCI rear panel connectors. J1 contains the 32-bit 66MHz PCI interface. J2 contains the two Camera Link interfaces as well as the opto-isolated, TTL and LVDS IO. The "Chain" functionality is incorporated into the J2 connector and allows two ***Phoenix*** boards to be used together to simultaneously acquire from wider sources. The next section shows the pinout of the connectors.

CONNECTOR PINOUTS

J2 Connector

Phoenix-D48CL is fitted with the J2 connector. It contains the two Camera Link channels, TTL, opto-isolated and EIA-644 I/O. An optional rear panel I/O adapter board (***AS-PHX-ADP-3CPCI-48CL-IO***) is available and provides convenient access to the various Camera Link ports and I/O signals.

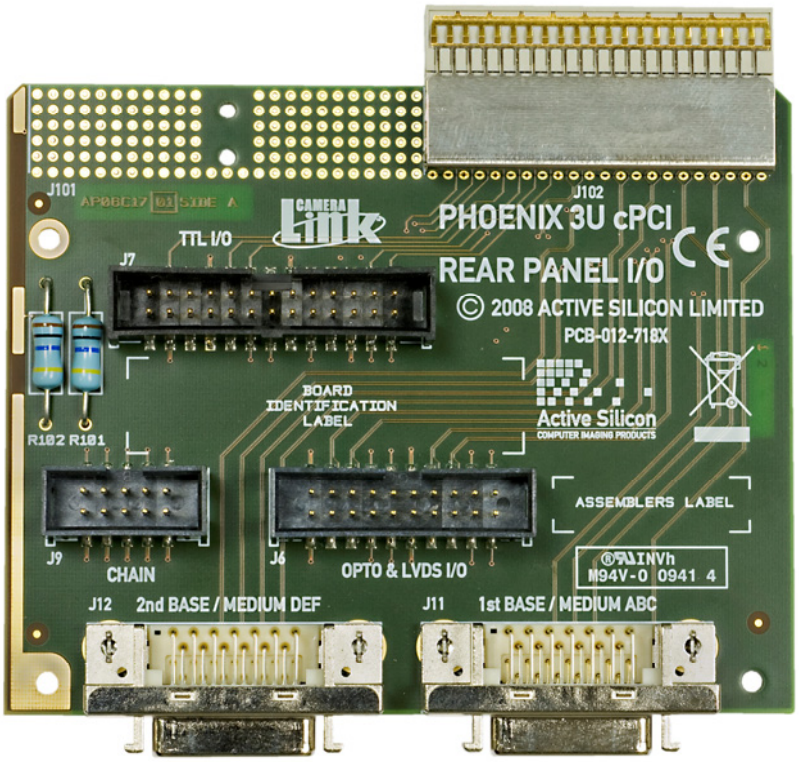
PIN	Z	A	B	C	D	E	F
1	GND	X1+	X1-	GND	X0+	X0-	GND
2	GND	XClk+	XClk-	GND	X2+	X2-	GND
3	GND	X3+	X3-	GND	GND	GND	GND
4	GND	XCC2+	XCC2-	GND	XCC1+	XCC1-	GND
5	GND	XCC4+	XCC4-	GND	XCC3+	XCC3-	GND
6	GND	XSerTFG+	XSerTFG-	GND	XSerTC+	XSerTC-	GND
7	GND	AuxIn A1+	AuxIn A1-	GND	AuxInB1+	AuxIn B1-	GND
8	GND	AuxIn A2+	AuxIn A2-	GND	AuxIn B2+	AuxIn B2-	GND
9	GND	Y0+	Y0-	GND	YCC1+	YCC1-	GND
10	GND	Y1+	Y1-	GND	YCC3+	YCC3-	GND
11	GND	Y3+	Y3-	GND	Y2+	Y2-	GND
12	GND	YCC2+	YCC2-	GND	YClk+	YClk-	GND
13	GND	YCC4+	YCC4-	GND	GND	GND	GND
14	GND	YSerTFG+	YSerTFG-	GND	YSerTC+	YSerTC-	GND
15	GND	GND	GND	GND	GND	GND	GND
16	GND	Chain 1	Chain 2	Chain 5	Chain 3	Chain 4	GND
17	GND	TTL B0	TTL B1	TTL B Len	TTL B2	TTL B3	GND
18	GND	TTL A0	TTL A1	TTL A Len	TTL A2	TTL A3	GND
19	GND	OptoA2 Sig	OptoA2 Cmn	GND	OptoB2 Sig	OptoB2 Cmn	GND
20	GND	OptoA1 Sig	OptoA1 Cmn	GND	OptoB1 Sig	OptoB1 Cmn	GND
21	GND	X Power	X Power	GND	Y Power	Y Power	GND
22	GND	NC	NC	NC	NC	NC	NC

NOTES:

1. For clarity, the Camera Link pinout shown is for the dual Base configuration. In Medium configuration, the second Camera Link Base connector *Xn* signals are used as *Yn* inputs, and the *CCn* and *Ser* I/O signals are not used.
2. The naming convention used is standard bit ordering, i.e. TTL A0 and TTL A7 are the LSB and MSB bits respectively of TTL Port A.
3. TTL *X* Len is a latch enable signal for the appropriate port. If it is held at a logical "0", then the current values on the I/O port pins are read. If it is held at a logical "1", then the values on the I/O port pins when TTL *X* Len transitioned from "0" to "1" are read. By default, this signal is fitted with a 4.7kΩ pulldown resistor, such that it can be left unconnected.
4. The standard build of ***Phoenix-D48CL*** provides two opto-isolated inputs (OptoA1 & OptoB1) and two opto-isolated outputs (OptoA2 & OptoB2). These can be supplied with other combinations of input or output - please consult your distributor for more information.
5. The opto-isolated outputs are designed to sink up to 20mA of current from a 24V supply, and the inputs sense voltages between 3.3V and 24V as a logic high input.
6. AuxIn*XY* are EIA-644 (LVDS) inputs used to connect external devices such as shaft encoders, or other trigger devices.

Rear Panel I/O Adapter (optional item)

An interface adapter (***AS-PHX-ADP-3CPCI-48CL-IO***) is available which utilises the rear panel I/O slot to access the Camera Link and I/O signals. This adapter connects to the J2 connector (via a suitable backplane) on the ***Phoenix-D48CL***. The below picture shows Camera Link and I/O connectors located on the adapter.



Camera Connectors

Phoenix-D48CL is fitted with two 26 way mini-D Camera Link sockets on the PCI end bracket.
Connector type: 3M MDR (N10226-52B2VC) with 3M screwlocks (3341-31).

PIN	SIGNAL	PIN	SIGNAL
1	Inner Shield (Power)	14	Inner Shield (Return)
2	CC4-	15	CC4+
3	CC3+	16	CC3-
4	CC2-	17	CC2+
5	CC1+	18	CC1-
6	SerTFG+	19	SerTFG-
7	SerTC-	20	SerTC+
8	X3+	21	X3-
9	XClk+	22	XClk-
10	X2+	23	X2-
11	X1+	24	X1-
12	X0+	25	X0-
13	Inner Shield (Return)	26	Inner Shield (Power)

NOTES:

1. For clarity, the Camera Link pinout shown is for the Base configuration. In Medium configuration, the second Camera Link Base connector *Xn* signals are used as *Yn* inputs, and the *CCn* and *Ser* I/O signals are not used.
2. Names in parenthesis are those used by Power over Camera Link (PoCL)

TTL I/O Connector

Phoenix ADP-3CPCI-48CL-IO is fitted with a 26 way header for TTL I/O.
Connector type: Standard 26 way 0.1" pitch box header for use with IDC sockets.

PIN	SIGNAL	PIN	SIGNAL
1	TTL A0 (*LSB*)	2	TTL A1
3	TTL A2	4	TTL A3
5	NC	6	GND
7	NC	8	NC
9	NC	10	TTL A Len
11	GND	12	NC
13	NC	14	TTL B0 (*LSB*)
15	TTL B1	16	TTL B2
17	TTL B3	18	NC
19	GND	20	NC
21	NC	22	NC
23	TTL B Len	24	GND
25	NC	26	NC

NOTES:

1. The naming convention used is standard bit ordering, i.e. TTL A0 and TTL A3 are the LSB and MSB bits respectively of TTL Port A.
2. TTL *X* Len is a latch enable signal for the appropriate port. If it is held at a logical "0", then the current values on the I/O port pins are read. If it is held at a logical "1", then the values on the I/O port pins when TTL *X* Len transitioned from "0" to "1" are read. By default, this signal is fitted with a 4.7kΩ pulldown resistor, such that it can be left unconnected.

Opto-Isolated & EIA-644 I/O Connector

Phoenix ADP-3CPCI-48CL-IO is fitted with a 20 way header for opto-isolated and EIA-644 I/O.
Connector type: Standard 20 way 0.1" pitch box header for use with IDC sockets.

PIN	SIGNAL	PIN	SIGNAL
1	OptoA1 Signal	2	OptoA1 GND
3	OptoA2 Signal	4	OptoA2 GND
5	AuxInA1+	6	AuxInA1-
7	AuxInA2+	8	AuxInA2-
9	GND	10	GND
11	OptoB1 Signal	12	OptoB1 GND
13	OptoB2 Signal	14	OptoB2 GND
15	AuxInB1+	16	AuxInB1-
17	AuxInB2+	18	AuxInB2-
19	GND	20	GND

NOTES:

1. The opto-isolated I/O consists of a signal and a ground connection, all of which are all isolated from each other and the main GND signal.
2. The standard build of ***Phoenix-D48CL*** provides two opto-isolated inputs (OptoA1 & OptoB1) and two opto-isolated outputs (OptoA2 & OptoB2). These can be supplied with other combinations of input or output - please consult your distributor for more information.
3. The opto-isolated outputs are designed to sink up to 20mA of current from a 24V supply, and the inputs sense voltages between 3.3V and 24V as a logic high input.
4. AuxIn*XY* are EIA-644 (LVDS) inputs used to connect external devices such as shaft encoders, or other trigger devices.

CONFORMANCE

PCI Interface:	PCI (Peripheral Component Interconnect) Bus to PCI Local Bus Specification Revision 2.2. ***Phoenix-D48CL*** implements a 32 bit 66MHz interface, supporting 3.3V only. ***Phoenix-D48CL*** is Bus Master capable with 0 wait states, thus achieving burst rates of 266MBytes/sec in a 32 bit 66MHz slot, subject to host performance. The board is automatically mapped into memory space, requiring 16 MBytes of address range, and drives "IntA" interrupt output.
CompactPCI:	***Phoenix-D48CL*** conforms to CompactPCI Specification PCIMG 2.0 R3.0. As standard it does not support the optional Hot Swap or System Management extensions.
Camera Link:	***Phoenix-D48CL*** conforms to v1.2 of the Camera Link specification.
Approvals:	EU CE mark for compliance with EMC EN 55022:1998 (class A) and EN 55024:1998 in accordance with EU directive 89/336/EEC. RoHS Compliant. USA EMC FCC Class A. The printed circuit board is manufactured by UL recognised manufacturers and has a flammability rating of 94-V0.

PHYSICAL AND ENVIRONMENTAL DETAILS

Dimensions:	PCB: 160mm by 100mm. Overall: 167mm by 100mm.	
Approximate weight:	106g. 180g (including conduction cooled assembly).	
Power consumption (typical): *(PCI32M66)*	+3.3V 600mA	+12V 50mA (PoCL control) plus up to 8W (for PoCL cameras).
Storage Temperature:	-40°C to +85°C.	
Operating Temperature:	-40°C to +85°C.	
Relative Humidity:	10% to 90% non-condensing (operating and storage).	

ORDERING INFORMATION

PART NUMBER	*DESCRIPTION*
AS-PHX-D48CL-3CPCI32-B-CR	Camera Link frame grabber for Base, Dual Base or Medium Camera Link configurations. PCI bus with 32 bit, 66MHz, 3.3V signalling. 3U CompactPCI form factor.
AS-MEC-CCA-3U-A	Optional conduction cooled assembly.
AS-PHX-SDK-xxx-CD	Software Development Kit for *xxx* operating system. For a full list of all supported operating systems please refer to the SDK datasheet, or contact your distributor.
AS-PHX-ADP-3CPCI-48CL-IO	Rear panel adapter for access to I/O and camera data, comprising 2 standard MDR Camera Link sockets, 20 and 26 way 0.1" IDC headers. Connects to the J2 connector on the rear panel backplane.

An initial order for ***Phoenix*** with an SDK is supplied in a presentation case.

THE PHOENIX RANGE

The following products are available in the Phoenix range:

- CoaXPress frame grabbers.
- Base only Camera Link frame grabber.
- Base, Dual Base and Medium Camera Link frame grabber.
- Base, Medium and Full Camera Link frame grabber.
- 36 bit LVDS frame grabber.
- HD-SDI frame grabber.

They are available in standard PCI Express, PCI, PMC, CompactPCI, PCI/104-Express and PC/104-Plus form factors.

More products are in development. Please consult your distributor for information on the availability of other camera interface, PCI interface, and form factor options.

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