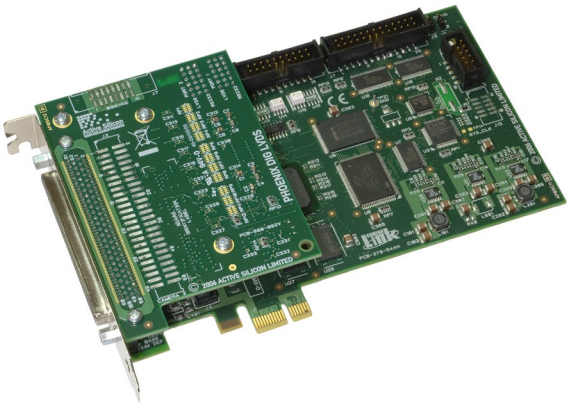
PHOENIX-D36 PCI EXPRESS

HIGH PERFORMANCE/HIGH SPEED DIGITAL FRAME GRABBER

- 36 bit EIA-644 (LVDS) data plus 4 bits for control.
- Single lane (x1) v1.1 PCI Express interface.
- PCI Express burst rates in excess of 190Mbytes/sec.
- Supports digital areascan / linescan cameras.
- Accepts multi-tap & multi-channel camera formats, including line and pixel interleaved.
- Maximum pixel clock of 60MHz.
- Software Development Kit (SDK) supports various operating systems for rapid integration.
- Bus mastering hardware control of scatter-gather requires 0% host CPU intervention.
- Dual channel serial port with both EIA-232 & EIA-644 signalling.
- Opto-Isolated, TTL, EIA-644 (inputs) and EIA-422 (outputs).
- Utilises software configurable FPGA technology for maximum flexibility.
- Common API allows seamless migration for existing Phoenix PCI users.
- RoHS compliant.



Active Silicon
COMPUTER IMAGING PRODUCTS

OVERVIEW

Phoenix-D36 is a PCI Express board for the acquisition of digital data from a variety of sources, including digital frame capture and line scan cameras. It has 36 bits used for input data, with 4 bits for control. This provides support for a single 12-bit RGB or 32-bit mono data source, including multi-tap cameras. The 4-bit control inputs are dedicated as Frame Enable, Line Enable, Data Enable and Pixel Clock. Alternatively, four of the data inputs can be re-assigned as an additional control port, thus allowing two independent 16-bit mono cameras to be supported. Data widths up to the above maximums are also handled, i.e. 8, 10 or 12-bit RGB and 8, 10, 12, 14, 16 or 32-bit mono.

Phoenix-D36 also supports various camera tap formats, such as line interlaced - adjacent lines are output simultaneously; line offset - lines are output from different parts of the CCD simultaneously; pixel interlaced - adjacent pixels on the same line are output simultaneously; and pixel offset - pixels are output from different parts of the same line simultaneously.

ROI and sub-sampling controls are used to increase application processing speed by only storing the required data. In addition, the LUT functionality provides support for gamma correction, dynamic range cropping and binary thresholding in real time. The DataMapper further reduces the load on the host processor by mapping and packing the acquired data prior to transfer across the PCI Express bus. For example, the acquired data can be mapped into a suitable format and transferred directly to the graphics display, without the need for any host processing.

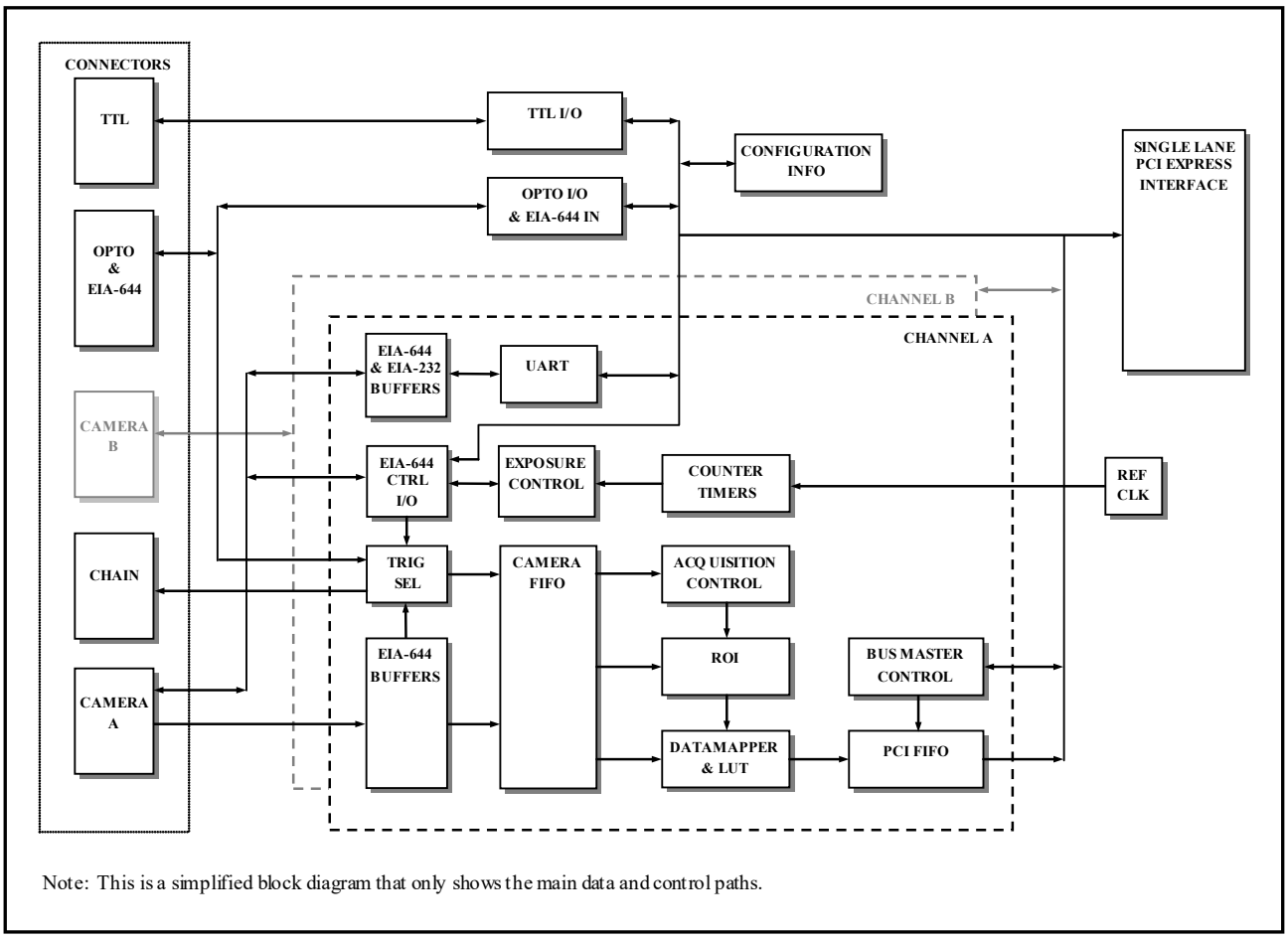
The PCI interface comprises intelligent scatter-gather hardware which reads its instructions direct from memory without any host CPU intervention. This in turn controls the DMA engine, which transfers the packed video data into any target memory which can be reached from the PCI Express bus. This can be system memory, graphics memory, or even other devices on the same or other PCI busses, such as DSP cards, etc.

The majority of the functionality is implemented in a single FPGA (Field Programmable Gate Array) providing a flexible solution for interfacing to digital sources. The FPGA implements the PCI Express interface, hardware scatter-gather control of DMA, Acquisition Control, Region of Interest (ROI) and sub-sampling control, DataMapping functions, Datapath FIFOs, and Counter/Timer support. In addition the board contains Look Up Table (LUT) functionality, a dual Universal Asynchronous Receiver Transmitter (UART) with support for EIA-232 (RS-232) and EIA-644 (LVDS) levels, 4 bit opto-isolated I/O, two 2 bit differential input ports and two 8 bit TTL I/O ports.

The PHX Software Development Kit (SDK), available as a separate item, allows rapid system development and integration. It provides comprehensive example applications and optimized libraries, and is available for a variety of operating systems via a common API, including 32 bit and 64-bit versions of Windows and Linux as well as Mac OS X, QNX. Drivers for third party applications are also available, e.g. Common Vision Blox, Image-Pro Plus, StreamPix,

LabVIEW, MATLAB etc. As well as functions that control the hardware, the libraries include general purpose functions for the manipulation and display of images. A separate datasheet describes the SDK in detail.

SYSTEM BLOCK DIAGRAM



Note: This is a simplified block diagram that only shows the main data and control paths.

HARDWARE SPECIFICATION

Data Input:	***Phoenix*** has two dedicated 20-bit EIA-644 (LVDS) input channels each consisting of 16 bits of data and 4 bits of control (Frame Enable, Line Enable, Data Enable and Camera Clock). Each channel can be used to acquire 8, 10, 12, 14 or 16 bits of data, or two 8 bit taps from a single video source (In this mode the two taps must contain data from adjacent pixels within the same scan line, i.e. Tap #1 contains odd pixels & Tap #2 even pixels, or vice versa). The two channels can be used independently allowing simultaneous acquisition from two non-synchronised cameras (Dual Camera Mode). Alternatively, the channels can be combined into one wide channel consisting of 36 bits of data and 4 bits of control (Frame Enable, Line Enable, Data Enable and Camera Clock). This allows 12-bit RGB (i.e. 36 bits of data) or up to 32 bit mono to be acquired, as well as supporting two tap cameras where the data pixels are not adjacent, i.e. line interleaved cameras such as the Redlake ES4, etc. The various modes are selected under software control without the need for any hardware jumpers etc. Due to the termination method used, ***Phoenix*** accepts data from EIA-644 data sources, as well as many EIA-422 or EIA-485 ones.
Camera Clock:	***Phoenix*** supports clock rates from DC to 60MHz. For faster speeds contact your distributor. Each channel has a dedicated EIA-644 (LVDS) pixel clock input, with software programmable polarity.
Frame & Line Enables:	In areascan mode, both these control inputs are used to determine when the camera is outputting valid data. In linescan mode only the Line Enable signal is required, and Frame Enable can be connected as an additional trigger source.
Data Enable:	The Data Enable signal is a general purpose real time input, which can either be used to enable the actual camera data, as a Field ID flag for interlaced cameras, or a trigger input.
Camera FIFO:	Data from the video source is stored in a FIFO prior to being processed by ***Phoenix***. This allows the camera clock to be stopped and started, whilst only requiring a single active camera clock before or after any change of the control signals, i.e. Frame Enable, Line Enable or Data Enable. For certain high bandwidth applications, it is possible to extend the FIFO size - please contact your distributor for more details.
Acquisition Control:	The acquisition trigger control module is used to determine which video frames to acquire from the camera. The system can be configured for a single trigger event to acquire all subsequent frames, a trigger event per frame, or continuous acquisition irrespective of the trigger condition. The trigger event is programmable between level or edge sensing on one of the opto-isolated or EIA-644 control inputs. When running in linescan mode, there is an additional mode that uses the active trigger input as an envelope signal. In this mode all lines are acquired whilst the trigger input is asserted. The hardware can also delay the trigger event by a fixed time period or number of lines, and allows the trigger event transducer to be located remotely from the camera.
Region of Interest:	The Region Of Interest (ROI) controls which part of the camera output data to acquire. In areascan mode, this is a rectangular region with software programmable width, height and x / y offset. Linescan mode is similar, allowing control of the width and x offset, with the height control being used to package the data into pseudo frames for subsequent processing by the user's application. ***Phoenix*** supports an additional mode (DataStream) whereby data is acquired based upon the control inputs, e.g. all data is acquired when Frame Enable and Line Enable are both asserted. This is necessary for cameras that output their own arbitrary ROIs within a single video frame, or those that vary the amount of data output on each line.
Sub-Sampling:	Software controlled hardware sub-sampling is also supported. A factor of x1, x2, x4 or x8 can be independently selected for both x and y directions, e.g. a horizontal factor of x4 and a vertical factor of x2 would acquire every 4th pixel across a line and every 2nd line down the frame.

DataMapper:	The raw camera data can be reformatted in hardware for ease of subsequent processing. For example, a mono data source can be converted into 32-bit color data, ready to be sent directly to graphics card memory, thus reducing the host processor overhead. The optimum use of system resources is determined by the user's application, e.g. packing mono data into 32-bit color reduces the host processor overhead at the expense of increasing the amount of data transferred across the PCI Express bus. The output formats supported include, 8, 16 and 32-bit mono, as well as 15, 16, 24, 32 and 48 bit color in both RGB and BGR ordering, thus supporting big and little endian processor formats.
LUT:	A 16 bit in, 16-bit out (i.e. 65,536 by 16) LUT per channel allows arbitrary mappings between the input data from the video source and the output data to the destination memory. This allows functions such as gamma correction, brightness, contrast and thresholding to be performed in real time in hardware on a per color or per camera basis. The LUT may also be used to shift the MSB aligned video data to LSB alignment ready for processing.
PCI FIFO:	A 4096 by 32-bit FIFO provides buffering between the camera and the PCI Express bus, as well as packet buffering in the PCI Express interface. Note that this is not a frame store; ***Phoenix*** uses high speed DMA to transfer the camera data into system memory, and therefore the image size is only limited by the amount of memory available on the host.
Bus Master Control:	Core to ***Phoenix*** is a dedicated RISC processor and a highly optimised DMA engine. The RISC processor generates PCI Express Non-Posted requests to system memory to read transfer length, destination address and other control information directly from host memory. For optimal efficiency, the resulting instructions are held in a pipeline buffer before being used to generate Posted packets containing image data. The RISC processor optionally generates a PCI interrupt to signal that the transfer has completed, before continuing to execute the next instruction, and also supports jump instructions that allow a single piece of RISC code to loop continuously. This whole process is completely autonomous to the hardware and requires 0% CPU overhead to maintain. The DMA engine is thus capable of sending data at the full PCI Express rate and the throughput is only limited by the max payload size of the host machine.
Interrupts:	An interrupt signal is available, and can be configured via software to interrupt on a number of different events, including acquisition complete, FIFO overflow, Start/End of Frame/Line, etc.
Serial Port:	***Phoenix*** is fitted with a dual channel Universal Asynchronous Receiver Transmitter (UART), containing 64-character hardware transmit and receive FIFOs for each channel (the software libraries buffer the transmit and receive data to provide larger user FIFOs). Each channel independently supports 1, 1.5 or 2 stop bits; 5, 6, 7 or 8 data bits; and odd, even or no parity. The baudrate can be configured with standard values from 300 baud up to 115,200 baud. ***Phoenix*** also supports software (XON, XOFF) flow control within the UART without host CPU intervention. Hardware jumpers are provided to select between EIA-644 and EIA-232 (RS-232) signalling levels. In EIA-232 mode RTS, CTS, TX and RX are all supported. In EIA-644 mode TX and RX are supported for both channels, or under software control, RTS, CTS TX and RX can be supported for a single channel of the UART. Note that TX and RTS are ***Phoenix*** outputs; RX and CTS are ***Phoenix*** inputs.

Counter Timers:	Four 32-bit counter timers are available for each channel of the ***Phoenix***. The counter timers are dedicated for the following functions: 1. Astable timer used as a line rate generator for linescan cameras, or as an acquisition trigger for areascan cameras, thus controlling the overall frame rate. The period of the astable can be set from 1µs up to 70 minutes in 1µs increments. 2. Dual monostables for generating two exposure output signals, e.g. ExSync and PRIN. Both monostables are triggered by the same software selectable event but can be programmed with different time periods, once again to 1µs resolution. This provides a flexible exposure control system. 3. Trigger delay counter used to postpone acquisition triggering by a programmable time delay or line count. This allows the acquisition trigger sensor to be mounted remotely from the camera. (Note: As the counter is non-retriggerable, subsequent trigger events will be ignored until a pending event has completed its delay). 4. A versatile event counter is provided to count a number of different events types - Lines, Frames or microseconds, within a specified gate condition - Line, Frame, Acquisition Trigger or Entire Acquisition. The event count provides readings for both the current value, as well as the final value at the end of the previous gate condition. For example, the event counter can be configured to provide the current line number within a frame, as well as the total number of lines in the previous frame. Other uses include providing the frame period, the number of lines in the previous acquisition trigger envelope – and hence how much data there is to process, or the number of images processed so far.
Opto-Isolated I/O:	4 bits of opto-isolated I/O are provided to interface to external systems. As standard, ***Phoenix*** is configured with 2 bits of input and 2 bits of output, but this can be varied as factory build option - please contact your distributor for further information. The outputs are designed to sink up to 20mA, and will withstand 24V when “off”. The inputs sense voltages between 3.3V and 24V as a logic high input. A 4.7kΩ current limiting series resistor is fitted on all inputs. The outputs can be individually set and cleared via software, controlled from the internal timer resources, or fed from other input events, e.g. acquisition triggers, etc.
EIA-644 Control In:	Two 2-bit EIA-644 (LVDS)input ports are provided to interface with other systems. They can be used to read status information from the camera, as additional acquisition trigger sources, or as inputs from shaft encoders, etc.
TTL I/O:	Two 8-bit TTL I/O ports are provided to interface with other systems. Each 8 bit port can be independently configured as all input or all output under software control. When used as outputs, each bit can source 24mA at min 2.2V or sink 24mA at max 0.55V. When used as inputs, an applied voltage of between 2V and 5V is read as a logical “1” and an applied voltage of between 0V and 0.8V as a logical “0”.
Connectors:	***Phoenix*** is fitted with a 100-way mini-D connector that provides all the necessary interface signals to connect to the camera. In addition, an optional internal 50 way 0.1” IDC header provides access to half the signals. This is intended for use in Dual Camera Mode and allows a standard camera cable (i.e. with a 100-way connector) to be used via the optional second camera adapter ***AS-PHX-ADP-100MD-CAM*** to an adjacent PCI slot. Please contact your distributor for more details. For opto-isolated, EIA-644 & TTL I/O there are internal 20 & 26 way 0.1” IDC headers, with the option to bring these out to a 50-way mini D on an adjacent PCI slot. These can allow simplified cabling by keeping external I/O signals completely separate from camera signals, rather than needing to make a complex cable that splits to multiple connectors. A 10 way 0.1” IDC header (“Chain”) allows two ***Phoenix*** boards to be used together to simultaneously acquire from wider sources. The next section shows the pinout of the connectors.

CONNECTOR PINOUTS

Camera Connector

Phoenix-D36 is fitted with a 100-way mini-D connector on the PCI end bracket.
Connector type: 100 way mini-D pin-type connector (as HiPPI standard), Honda part PCS-XE100LFD-HS with 4-40UNC thread screwlocks. The cable mounted mating part is Honda PCS-XE100MA, with hood PCS-XEM100L.

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	MSB-16+	26	MSB-28+	51	MSB+	76	MSB-12+
2	MSB-16-	27	MSB-28-	52	MSB-	77	MSB-12-
3	MSB-17+	28	MSB-29+	53	MSB-1+	78	MSB-13+
4	MSB-17-	29	MSB-29-	54	MSB-1-	79	MSB-13-
5	MSB-18+	30	MSB-30+	55	MSB-2+	80	MSB-14+
6	MSB-18-	31	MSB-30-	56	MSB-2-	81	MSB-14-
7	MSB-19+	32	MSB-31+	57	MSB-3+	82	MSB-15+
8	MSB-19-	33	MSB-31-	58	MSB-3-	83	MSB-15-
9	MSB-20+	34	GND	59	MSB-4+	84	GND
10	MSB-20-	35	CtrlInB1+	60	MSB-4-	85	CtrlInA1+
11	MSB-21+	36	CtrlInB1-	61	MSB-5+	86	CtrlInA1-
12	MSB-21-	37	CtrlInB2+	62	MSB-5-	87	CtrlInA2+
13	MSB-22+	38	CtrlInB2-	63	MSB-6+	88	CtrlInA2-
14	MSB-22-	39	CtrlInB3+	64	MSB-6-	89	CtrlInA3+
15	MSB-23+	40	CtrlInB3-	65	MSB-7+	90	CtrlInA3-
16	MSB-23-	41	CtrlInB4+	66	MSB-7-	91	CtrlInA4+
17	GND	42	CtrlInB4-	67	GND	92	CtrlInA4-
18	MSB-24+	43	CcIoB1+	68	MSB-8+	93	CcIoA1+
19	MSB-24-	44	CcIoB1-	69	MSB-8-	94	CcIoA1-
20	MSB-25+	45	CcIoB2+	70	MSB-9+	95	CcIoA2+
21	MSB-25-	46	CcIoB2-	71	MSB-9-	96	CcIoA2-
22	MSB-26+	47	CamRx2+	72	MSB-10+	97	CamRx1+
23	MSB-26-	48	CamRx2-	73	MSB-10-	98	CamRx1-
24	MSB-27+	49	CamTx2+	74	MSB-11+	99	CamTx1+
25	MSB-27-	50	CamTx2-	75	MSB-11-	100	CamTx1-

NOTES:

1. The data bit naming convention used is “bits below the Most Significant Bit (MSB)” with the “-” standing for “minus”, i.e. “MSB-7” is seven bits below the MSB, which in the case of an 8 bit mono camera is the Least Significant Bit (LSB). This follows the American Imaging Association (AIA) naming convention.
   Important: Always align the camera’s most significant bit with “MSB” and work down through the data signals.
2. Input Channel A connects to pins 51..100 using data bits MSB-[0:15], and Input Channel B connects to pins 0..50 using data bits MSB-[16:31].
3. CtrlIn*X*1 is Frame Enable (areascan) or an additional trigger (linescan), CtrlIn*X*2 is Line Enable, CtrlIn*X*3 is Data Enable or Field Flag, CtrlIn*X*4 is Camera Clock.
4. When the two channels are combined into one wide channel, CtrlInB1 to CtrlInB4 are used as data inputs MSB-[32:35].

5. For RGB cameras, Red inputs are in the range MSB-[0:11], Green in the range MSB-[12:23] and Blue in the range MSB-[24:35].
6. For two tap 8 bit cameras where the taps contain data from adjacent pixels within the same scan line, use MSB-[0:7] for the odd tap, and MSB-[8:15] for the even tap.
7. For two tap cameras of greater than 8 bits, or where the taps contain data pixels that are not adjacent, use MSB-[0:15] for the odd tap, and MSB-[16:31] for the even tap.
8. *C*cIoA1 & CcIoB1 can be used for ExSync, and CcIoA2 & CcIoB2 for PRIN.
9. In EIA-232 mode Camera RX, CTS, TX & RTS are connected to CamRx+, CamRx-, CamTx+ & CamTx- respectively for each port. In full EIA-644 mode, Camera RX, CTS, TX & RTS are connected to CamRx1, CamRx2, CamTx1 & CamTx2 respectively (refer to the Serial Port section).
10. Example camera connections follow. These are not intended to show valid connections for any specific cameras, but to clarify these notes by showing typical connections.

Example: Minimal Connections for a 10 Bit Mono Area Scan Camera

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	-	26	-	51	D9+ (MSB)	76	-
2	-	27	-	52	D9-	77	-
3	-	28	-	53	D8+	78	-
4	-	29	-	54	D8-	79	-
5	-	30	-	55	D7+	80	-
6	-	31	-	56	D7-	81	-
7	-	32	-	57	D6+	82	-
8	-	33	-	58	D6-	83	-
9	-	34	-	59	D5+	84	GND
10	-	35	-	60	D5-	85	Frame+
11	-	36	-	61	D4+	86	Frame-
12	-	37	-	62	D4-	87	Line+
13	-	38	-	63	D3+	88	Line-
14	-	39	-	64	D3-	89	-
15	-	40	-	65	D2+	90	-
16	-	41	-	66	D2-	91	Clock+
17	-	42	-	67	GND	92	Clock-
18	-	43	-	68	D1+	93	-
19	-	44	-	69	D1-	94	-
20	-	45	-	70	D0+ (LSB)	95	-
21	-	46	-	71	D0-	96	-
22	-	47	-	72	-	97	-
23	-	48	-	73	-	98	-
24	-	49	-	74	-	99	-
25	-	50	-	75	-	100	-

Example: Typical 36 Bit RGB Area Scan Camera with EIA-644 Serial Port

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	G7+	26	B7+	51	R11+ (MSB)	76	G11+ (MSB)
2	G7-	27	B7-	52	R11-	77	G11-
3	G6+	28	B6+	53	R10+	78	G10+
4	G6-	29	B6-	54	R10-	79	G10-
5	G5+	30	B5+	55	R9+	80	G9+
6	G5-	31	B5-	56	R9-	81	G9-
7	G4+	32	B4+	57	R8+	82	G8+
8	G4-	33	B4-	58	R8-	83	G8-
9	G3+	34	GND	59	R7+	84	GND
10	G3-	35	B3+	60	R7-	85	V Sync+
11	G2+	36	B3-	61	R6+	86	V Sync-
12	G2-	37	B2+	62	R6-	87	H Sync+
13	G1+	38	B2-	63	R5+	88	H Sync-
14	G1-	39	B1+	64	R5-	89	TriggerIn+
15	G0+ (LSB)	40	B1-	65	R4+	90	TriggerIn-
16	G0-	41	B0+ (LSB)	66	R4-	91	Clock+
17	GND	42	B0-	67	GND	92	Clock-
18	B11+ (MSB)	43	-	68	R3+	93	-
19	B11-	44	-	69	R3-	94	-
20	B10+	45	-	70	R2+	95	-
21	B10-	46	-	71	R2-	96	-
22	B9+	47	CTS+	72	R1+	97	RX+
23	B9-	48	CTS-	73	R1-	98	RX-
24	B8+	49	RTS+	74	R0+ (LSB)	99	TX+
25	B8-	50	RTS-	75	R0-	100	TX-

Example: Two Line Scan Cameras: Camera A is 14 bit; Camera B is two tap 8 bit

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	Odd7+ (MSB)	26	Even3+	51	D13+ (MSB)	76	D1+
2	Odd7-	27	Even3-	52	D13-	77	D1-
3	Odd6+	28	Even2+	53	D12+	78	D0+ (LSB)
4	Odd6-	29	Even2-	54	D12-	79	D0-
5	Odd5+	30	Even1+	55	D11+	80	-
6	Odd5-	31	Even1-	56	D11-	81	-
7	Odd4+	32	Even0+ (LSB)	57	D10+	82	-
8	Odd4-	33	Even0-	58	D10-	83	-
9	Odd3+	34	GND	59	D9+	84	GND
10	Odd3-	35	-	60	D9-	85	-
11	Odd2+	36	-	61	D8+	86	-
12	Odd2-	37	LVAL+	62	D8-	87	Line Valid+
13	Odd1+	38	LVAL-	63	D7+	88	Line Valid-
14	Odd1-	39	DVAL+	64	D7-	89	-
15	Odd0+ (LSB)	40	DVAL-	65	D6+	90	-
16	Odd0-	41	Pixel Clock+	66	D6-	91	Strobe+
17	GND	42	Pixel Clock-	67	GND	92	Strobe-
18	Even7+ (MSB)	43	-	68	D5+	93	ExSync+
19	Even7-	44	-	69	D5-	94	ExSync-
20	Even6+	45	-	70	D4+	95	PRIN+
21	Even6-	46	-	71	D4-	96	PRIN-
22	Even5+	47	RX+	72	D3+	97	RX+
23	Even5-	48	RX-	73	D3-	98	RX-
24	Even4+	49	TX+	74	D2+	99	TX+
25	Even4-	50	TX-	75	D2-	100	TX-

TTL I/O Connector

Phoenix-D36 is fitted with an internal 26-way header for TTL I/O.
Connector type: Standard 26 way 0.1" pitch box header for use with IDC sockets.

PIN	SIGNAL	PIN	SIGNAL
1 *(1)*	TTL A0 (*LSB*)	2 *(2)*	TTL A1
3 *(3)*	TTL A2	4 *(4)*	TTL A3
5 *(5)*	TTL A4	6 *(6)*	GND
7 *(7)*	TTL A5	8 *(8)*	TTL A6
9 *(9)*	TTL A7 (*MSB*)	10 *(10)*	TTL A Len
11 *(11)*	GND	12 *(12)*	CcIoA1 TTL
13 *(13)*	CcIoA2 TTL	14 *(26)*	TTL B0 (*LSB*)
15 *(27)*	TTL B1	16 *(28)*	TTL B2
17 *(29)*	TTL B3	18 *(30)*	TTL B4
19 *(31)*	GND	20 *(32)*	TTL B5
21 *(33)*	TTL B6	22 *(34)*	TTL B7 (*MSB*)
23 *(35)*	TTL B Len	24 *(36)*	GND
25 *(37)*	CcIoB1 TTL	26 *(38)*	CcIoB2 TTL

NOTES:

1. The naming convention used is standard bit ordering, i.e. TTL A0 and TTL A7 are the LSB and MSB bits respectively of TTL Port A.
2. TTL *X* Len is a latch enable signal for the appropriate port. If it is held at a logical "0", then the current values on the I/O port pins are read. If it is held at a logical "1", then the values on the I/O port pins when TTL *X* Len transitioned from "0" to "1" are read. By default, this signal is fitted with a 4.7kΩ pulldown resistor, such that it can be left unconnected.
3. CcIo*X* TTL are buffered output-only TTL versions of the CcIo*X* EIA-644 signals available on the front panel connector.
4. The pin numbers in parentheses are for the Combined I/O Adapter.

Opto-Isolated & EIA-644 I/O Connector

Phoenix-D36 is fitted with an internal 20-way header for opto-isolated and EIA-644 I/O.
Connector type: Standard 20 way 0.1" pitch box header for use with IDC sockets.

PIN	SIGNAL	PIN	SIGNAL
1 *(16)*	OptoA1 Signal	2 *(17)*	OptoA1 GND
3 *(18)*	OptoA2 Signal	4 *(19)*	OptoA2 GND
5 *(20)*	AuxInA1+	6 *(21)*	AuxInA1-
7 *(22)*	AuxInA2+	8 *(23)*	AuxInA2-
9 *(24)*	GND	10 *(25)*	GND
11 *(41)*	OptoB1 Signal	12 *(42)*	OptoB1 GND
13 *(43)*	OptoB2 Signal	14 *(44)*	OptoB2 GND
15 *(45)*	AuxInB1+	16 *(46)*	AuxInB1-
17 *(47)*	AuxInB2+	18 *(48)*	AuxInB2-
19 *(49)*	GND	20 *(50)*	GND

NOTES:

1. The opto-isolated I/O consists of a signal and a ground connection, all of which are all isolated from each other and the main GND signal.
2. The standard build of ***Phoenix-D36*** provides two opto-isolated inputs (OptoA1 & OptoB1) and two opto-isolated outputs (OptoA2 & OptoB2). These can be supplied with other combinations of input or output - please consult your distributor for more information.
3. The opto-isolated outputs are designed to sink up to 20mA of current from a 24V supply, and the inputs sense voltages between 3.3V and 24V as a logic high input.
4. AuxIn*XY* are EIA-644 (LVDS) I/O used to connect external devices such as shaft encoders, or other trigger devices.

Combined I/O Adapter (optional item)

An interface adapter (***AS-PHX-ADP-50MD-IO***) is also available which utilises a free adjacent PCI slot to access all the I/O signals from the two internal 0.1" IDC headers. It consists of a single 50-way mini D connector (Honda part number "PCS-E50PM"), fitted with 4-40 UNC thread screwlocks, mounted on a PCI end bracket.

The pin numbers for this 50-way connector are in parentheses in the above tables.

CONFORMANCE

PCI Express Interface:	PCI Express Bus single lane interface to Specification Revision 1.1, with a max payload size of 512 bytes. ***Phoenix-D36*** supports both Short (32 bit) and Long (64 bit) Address packets for native 64 bit addressing. It also generates Posted Writes for image data, thus achieving transfer rates in excess of 190Mbytes/sec, subject to host performance. The board requires 16 MBytes of address space, and a further 256 bytes of I/O space	
Approvals:	EU	CE mark for compliance with EMC EN 55022:1998 (class A) and EN 55024:1998 in accordance with EU directive 89/336/EEC. RoHS Compliant
	USA	EMC FCC Class A.
	The printed circuit board is manufactured by UL recognised manufacturers and has a flammability rating of 94-V0.	

PHYSICAL AND ENVIRONMENTAL DETAILS

Dimensions:	PCB:	143mm by 111mm
	Overall:	174mm by 127mm including end bracket and connectors.
Approximate weight:	150g	
Power consumption (typical):	+3.3V 1A	
Storage Temperature:	-15°C to +70°C.	
Operating Temperature:	0°C to +55°C.	
Relative Humidity:	10% to 90% non-condensing (operating and storage).	

ORDERING INFORMATION

PART NUMBER	*DESCRIPTION*
AS-PHX-D36-PE1	LVDS frame grabber. PCI Express bus with single lane (x1) bus interface.
AS-PHX-CBL-CH-IDC-M08	Chaining cable to connect two adjacent ***Phoenix*** PCI boards.
AS-PHX-ADP-50MD-IO	Combined I/O adapter, comprising a PCI end bracket with a 50-way mini-D connector, ribbon cables to the internal 20 and 26 way 0.1" IDC headers, and a mating 50 way connector with hood.
AS-PHX-SDK-xxx-CD	Software Development Kit for *xxx* operating system. For a full list of all supported operating systems please refer to the SDK datasheet, or contact your distributor.

Cables are available to connect to many makes of camera. Please consult your distributor for details.
An initial order for ***Phoenix*** with an SDK is supplied in a presentation case.

THE PHOENIX RANGE

The following products are available in the Phoenix range:

- CoaXPress frame grabbers.
- Base only Camera Link frame grabber.
- Base, Dual Base and Medium Camera Link frame grabber.
- Base, Medium and Full Camera Link frame grabber.
- 36-bit LVDS frame grabber.

They are available in standard PCI Express, PCI, PMC, CompactPCI, PCI/104-Express and PC/104-Plus form factors.

More products are in development. Please consult your distributor for information on the availability of other camera interfaces, PCI interface, and form factor options.

Active Silicon
COMPUTER IMAGING PRODUCTS
A SOLID STATE PLC GROUP COMPANY

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