SPB228 – WLAN/BT5 2x2 MU-MIMO Module

Data Sheet

SPB228

802.11 ac/a/b/g/n
2x2 MU-MIMO
Bluetooth 5

H&D Wireless

Current revision: 12.0

Revision History

Revision	Revision date	Description
7.0	2017-11-23	Updated with current consumption figures
8.1	2018-02-27	Added the PCIe/USB firmware Updated drawings, layout guidelines
8.2	2018-05-09	Updated the design direction section Updated module PCB thickness
8.3	2018-06-21	Referring to the RED directive in the ETSI section
8.4	2018-07-03	Updated power tables, pad drawing and solder paste recommendation
8.5	2018-07-15	Changed max rating storage temp, added ordering information
8.7	2018-10-17	Added info about number of clients in AP mode, added regulatory information and updated performance figures.
8.8	2018-12-04	Minor updates in pad drawing.
8.9	2019-02-22	Update of the document after data sheet review. Key Features, Order information, Soldering-and Sales information were updated among other.
9.0	2019-03-15	Pin 1 position shown from top view. Added article 3 of RED in section 7.2.3.
10.0	2019-03-19	Corrected RFC1023 to RFC1042 in section 6.1.
11.0	2019-11-29	Table 5-1 revised. List of approved antennas in section 6.3.1 revised.
12.0	2019-11-29	Corrected gain figures for Molex antennas. Added cable length for Maglayers antenna.

Content

1 INTRODUCTION

1.1 Overview

SPB228 is a complete WLAN/BT-module with integrated EMC shield, ready for onboard integration in a hosted environment. SPB228 enables a cost efficient ultra-low power, high performance and feature rich client solution. It provides up to 866.7 Mbit/s data rate when operating in the 2x2 Multi-User MIMO OFDM mode and up to 11 Mbit/s data rate when operating in the DSSS/CCK mode.

SPB228 integrates RF, baseband/MAC, Bluetooth Package Engine, memory, RF filters, oscillator and EMC shield into a highly integrated and optimized module solution with high quality and reliability to a complete standalone solution with minimum need for external components.

This highly integrated solution is optimized for customer applications running on a Linux host.
The host interface supports PCIe, SDIO 3.0, USB and UART. Internal RAM comprises both code and data memory eliminating the need for external RAM, Flash or ROM memory interfaces. MAC address, trimming values etc. are stored in the on-board memory.

1.2 Key Features

- Support for 802.11 ac/a/b/g/n
- Dual band 2.4/5 GHz
- 2x2 MU-MIMO
- Industrial temp -40 to +85°C
- M.2 1216 sized solder down module
- Data Rates:
  - Up to 866.7 Mbps with 802.11ac on 80 MHz channel and dual spatial streams.
  - Full support for all 802.11a/b/g rates
- 802.11n support for MCS0 – MCS15 and MCS32, HT20 and HT40
- 802.11ac support for MCS0 – MCS9, N_{ss} = 1 and 2, VHT20, VHT40 and VHT80
- Supports 8 clients in micro AP mode
- Supports 64 clients in full AP mode over PCIe
- Open WEP, WPA/WPA2 encryption
- Bluetooth 5
- No external components
- Low power consumption including sleep and standby modes
- Supporting STA and AP simultaneous operation
- Operations on two different channels with DRCS
- Wi-Fi Direct Peer-to Peer
- Supports BT-WLAN coexistence and ISM-LTE coexistence
- Simultaneous WLAN and Bluetooth operation including BLE
- Extensive DMA hardware support for data flow to reduce CPU load.
- Advanced power management for optimum power consumption at varying load.
- External interfaces PCIe, 4-bit SDIO 3.0 or USB 3/2 for WLAN/BT and also UART for BT
- PCM audio for BT interface
- On-board High Frequency High Precision Oscillator 40MHz
- Small footprint 12 x 16 mm (192 mm2) 96-pin industry standard pinning
- Dual micro RF connectors
- RoHS Compliant

2 HARDWARE ARCHITECTURE

2.1 Block Diagram

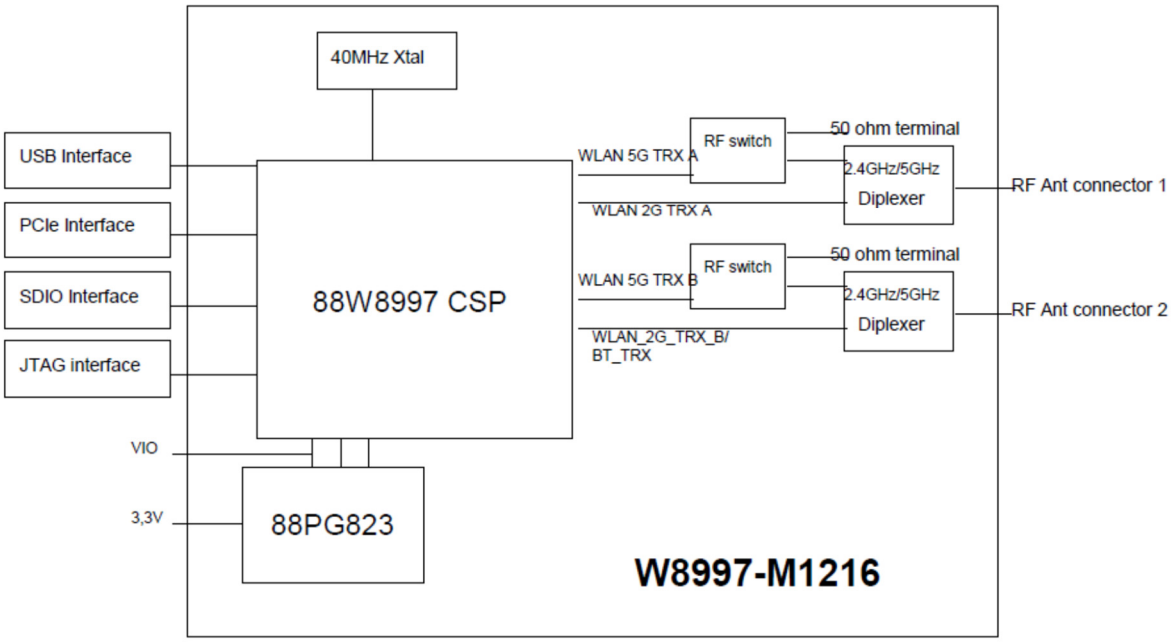

Figure 2-1: Block Diagram

2.2 Order information

SPB228-D SPB228 with dual RF micro connectors

Part No.	Description
SPB228-D-2	M.2 12x16mm solder down module on Tape&Reel
SPB228-D-3	M.2 12x16mm solder down module on Tray
HDA228-USB-SDIO	Development board for SPB228 platform, SD card format, USB and SDIO interface
HDA228-PCIE	Development board for SPB228 platform, PCIe card format, PCIE interface

3 ELECTRICAL DATA

3.1 Absolute maximum ratings

Rating	Min	Max	Units
Supply voltage	-0.3	4.0	V
Supply voltage I/O	-0.3	4.0	V
Input RF level		+10	dBm
Storage temperature	-55	+85	°C
Lead temperature (No Pb), solder as per section 5.6.3		+250	°C

Table 3-1: Absolute maximum ratings. Exceeding any of the maximum ratings, even briefly lead to deterioration in performance or even destruction. Values indicates condition applied one at the time.

3.2 Electro Static Discharge (ESD)

SPB228 withstands ESD voltages up to 1000V HBM (Human Body Model) per JESD22-A114 and up to 500 V CDM (Charged Device Model) according to JESD22-C101.

3.3 Recommended operating conditions

Rating	Min	Typ	Max	Units
Supply Voltage VDD33	3.0	3.3	3.47	V
Supply Voltage VIO_SD	1.62 or 2.97	1.8 or 3.3V	1.98 or 3.47	V
Supply Voltage VDDIO	1.62 or 2.25 or 2.97	1.8 or 2.5 or 3.3V	1.98 or 2.75 or 3.47	V
Supply Voltage IO with VDD 0V		0	0.2	V
Operating temperature	-40	+25	+85	°C

Table 3-2: Recommended operating conditions

3.4 Power Consumption

Conditions: VDD33=3.3V, T_{amb} = 25 °C
Power levels refer to total power on both antenna ports.

Mode	Conditions	Min	Typ.	Max	Units
2.4G/TX 802.11 b	DSSS 1Mbps, Pout=16 dBm, 1 path		340		mA
2.4G/TX 802.11 g	OFDM 6Mbps, Pout=16 dBm, 2 paths		490		mA

Mode	Conditions	Min	Typ.	Max	Units
2.4G/TX 802.11n HT40	OFDM MCS0, Pout=16 dBm		340		mA
5G/TX 802.11a	OFDM 6 Mbps, Pout=15 dBm		380		mA
5G/TX 802.11n HT40	OFDM MCS0, Pout=14 dBm		365		mA
5G/TX 802.11ac VHT80	OFDM MCS0, Pout=9 dBm, 2 paths		470		mA
2.4G/RX 802.11 g	Normal mode – 2 paths		108		mA
5G/RX 802.11a	Normal mode – 2 paths		130		mA
Continuous RX burst	SCO HV3 Peak RX		36		mA
Continuous Tx, +7 dBm	SCO HV3 Peak TX		48		mA
1.28 sec LE ADV			2		mA
1.28 sec sniff as master ACL Link			2		mA
Deep Sleep	Standby		800		µA
WLAN/Power Save	DTIM = 1, Beacon Interval 100ms, 2 paths		2.8		mA

Table 3-3: Typical current consumption in different modes.

3.5 RF Performance

Conditions: VDD33= 3.3V, T_{amb}= 25°C
Spectrum Mask and BER according to IEEE 802.11ac/a/b/g/n specification.
Power levels refer to total power on both antenna ports, same power on both ports.

Parameter	Conditions	Min	Typ.	Max	Units
2.4G/Frequency range		2412		2472	MHz
2.4G/Supported Channels	ETSI	Ch1 (2412 MHz)		Ch13 (2472 MHz)	
	FCC	Ch1 (2412 MHz)		Ch11 (2462 MHz)	
5G/Frequency range		4900		5925	MHz
5G/Supported Channels		Ch36 (5180 MHz)		Ch165 (5825MHz)	
RF impedance			50		Ohm
Transmitter performance, 11ac/a/b/g/n and BT					
2.4G/Output power	802.11b, 11Mbps		16		dBm
2.4G/Output power	802.11g, 54Mbps		16		dBm
2.4G/Output power	802.11n, MCS7 or MSC15, HT20		16		dBm
2.4G/Output power	802.11n, MCS7 or MSC15, HT40		16		dBm
5G/Output power	802.11a, 54Mbps		15		dBm

Parameter	Conditions	Min	Typ.	Max	Units
5G/Output power	802.11n, MCS7 or MSC15, HT20		14		dBm
5G/Output power	802.11n, MCS7 or MSC15, HT40		14		dBm
5G/Output power	802.11ac, MCS8, N_{ss} = 2, VHT20		14		dBm
5G/Output power	802.11ac, MCS9, N_{ss} = 2, VHT40		11		dBm
5G/Output power	802.11ac, MCS9, N_{ss} = 2, VHT80		10		dBm
BT BR	GFSK		6		dBm
BT EDR	π/4DQPSK & 8DPSK		3		dBm
BT LE			6		dBm
Receiver performance 11ac/a/b/g/n and BT, per Rx input					
2.4G/Receiver sensitivity	DPSK 1Mbit/s		-100		dBm
2.4G/Receiver sensitivity	OFDM/64-QAM 54Mbit/s		-77		dBm
2.4G/Receiver sensitivity	MCS-7, OFDM/64-QAM, HT20		-74		dBm
5G/Receiver sensitivity	OFDM/64-QAM 54Mbit/s		-74		dBm
5G/Receiver sensitivity	MCS-0, BPSK, HT20		-89		dBm
5G/Receiver sensitivity	MCS-9, OFDM/256-QAM, VHT40		-63		dBm
5G/Receiver sensitivity	MCS-0, BPSK, VHT80		-80		dBm
5G/Receiver sensitivity	MCS-9, OFDM/256-QAM, VHT80		-58		dBm
BT BR	GFSK, BER≤0.1%		-93		dBm
BT EDR	π/4DQPSK, BER≤0.1%		-94		dBm
BT EDR	8DPSK, BER≤0.1%		-88		dBm
BT LE	BER≤0.1%		-98		dBm

Table 3-4: RF Performance

3.6 Digital pin characteristics

3.6.1 SDIO timing characteristics

The SPB228 support a SDIO device interface that conforms to the industry standard SDIO 3.0 Full-speed specification and allows a host controller using the SDIO bus protocol to access the SPB228 device. SDIO-interface can run the SDIO 1-bit and 4-bit mode with full clock range up to 208MHz.

Condition: T_{amb}= -40 to +85°C

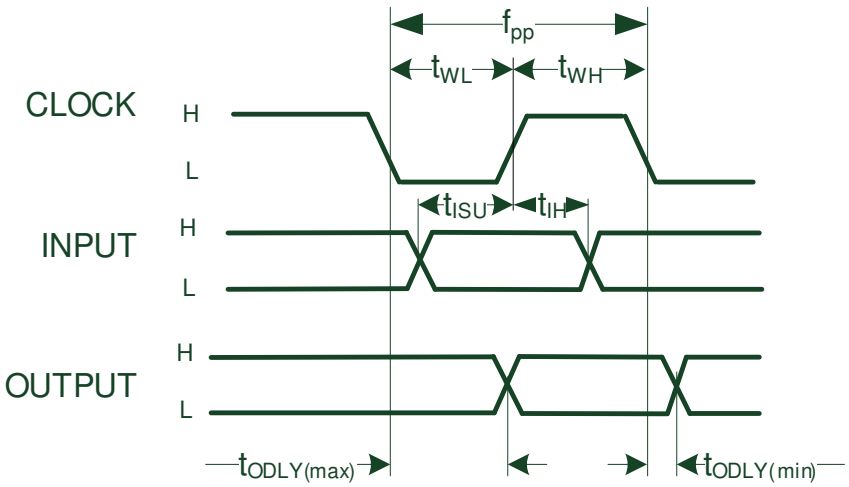

Figure 3-1: SDIO timing diagram

Parameter	Symbol	Min	Max	Units	Comments
Input set-up time	t_{ISU}	5		ns	
Input hold time	t_{IH}	5		ns	
Clock low time	t_{WL}	10		ns	
Clock high time	t_{WH}	10		ns	
Output delay time	t_{ODLY}		14	ns	
Clock Frequency	f_{pp}		25	MHz	

Table 3-5: SDIO timing parameter values (normal mode, VIO_SD = 1.8V or 3.3V)

Parameter	Symbol	Min	Max	Units	Comments
Input set-up time	t_{ISU}	6		ns	
Input hold time	t_{IH}	2		ns	
Clock low time	t_{WL}	7		ns	
Clock high time	t_{WH}	7		ns	
Output delay time	t_{ODLY}		14	ns	
Output hold time		2.5		ns	
Clock Frequency	f_{pp}		50	MHz	

Table 3-6: SDIO timing parameter values (high speed mode 50MHz, VIO_SD=1.8V highly recommended)

Parameter	Symbol	Min	Max	Units	Comments
Input set-up time	t_{ISU}	3		ns	
Input hold time	t_{IH}	0.8		ns	
Clock rise/fall time			0.2 / f_{pp}	ns	
Output delay time	t_{ODLY}		7.5	ns	
Output hold time	t_{OH}	1.5		ns	C_L = 15 pF
Clock Frequency	f_{pp}		100	MHz	

Table 3-7: SDIO timing parameter values (high speed mode 100MHz, VIO_SD= 1.8V)

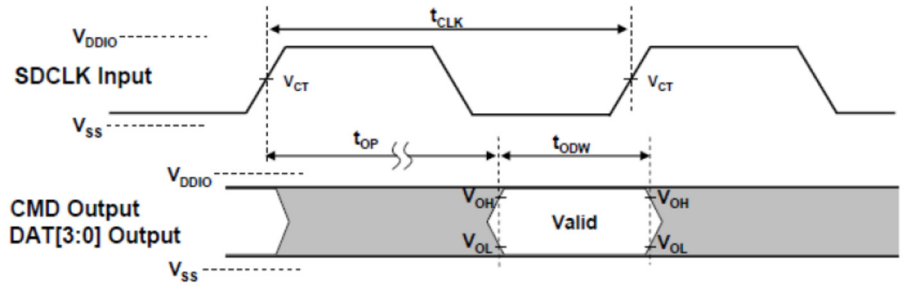

Figure 3-2: SDIO SDR104 output timing diagram

Parameter	Symbol	Min	Max	Units	Comments
Input set-up time	t_{ISU}	1.4		ns	
Input hold time	t_{IH}	0.8		ns	
Clock rise/fall time			0.2 / f_{pp}	ns	
Card Output Phase	t_{OP}	0	10	ns	
Output timing of variable data window	t_{ODW}	2.88		ns	
Clock Frequency	f_{pp}		208	MHz	

Table 3-8: SDIO timing parameter values (SDR104 mode 208MHz, VIO_SD= 1.8V)

3.6.2 PCI Express

The PCI Express host interface is internally powered with 1.8V.

Mode	Conditions	Min	Typ.	Max	Unit
Unit Interval	UI	399.88 199.94	400.12 200.06	ps	2.5GT/s 5GT/s
Differential peak-to-peak Tx voltage swing **$V_{Tx-DIFF-PP} = 2*\lvert V_{TD+} - V_{TD+}\rvert$**	$V_{Tx-DIFF-PP}$	0.8	1.2	V	
Low power differential peak-to-peak Tx voltage swing **$V_{Tx-DIFF-PP} = 2*\lvert V_{TD+} - V_{TD+}\rvert$**	$V_{Tx-DIFF-PP-LOW}$	0.4	1.2	V	
Tx deemphasis level ratio (3.5 dB)		3.0	4.0	dB	
Instantaneous lone pulse width, measured relative to rising/falling pulse		0.9		UI	
Tx eye including all jitter sources		0.75		UI	
Maximum time between jitter median and maximum deviation from median			0.125	UI	2.5GT/s
Tx deterministic jitter > 1.5 MHz			0.15	UI	5GT/s
Tx RMS jitter < 1.5 MHz			3.0	ps	5GT/s Typical value
Tx rise/fall time, measured differentially from 20% to 80% swing		0.125 0.15		UI	2.5GT/s 5GT/s
Tx package plus Si differential return loss		10 8		dB	2.5GT/s 5GT/s
Tx package plus Si common mode return loss		6		dB	
Tx AC common mode voltage			20	mV	2.5GT/s Typical value
Maximum Tx AC common mode voltage			100	mVpp	5GT/s
Tx short circuit current limit			90	mA	
Tx DC common mode voltage		0	3.6	V	
Absolute delta of DC common mode voltage during L0 and electrical idle		0	100	mV	
AC electrical idle differential peak output voltage		0	20	mV	
DC electrical idle differential peak output voltage		0	5	mV	
Voltage change allowed during receiver detection			600	mV	
Minimum time spent in electrical idle		20		ns	

Mode	Conditions	Min	Typ.	Max	Unit
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			8	ns	
Maximum time to transition to valid diff signaling after leaving electrical idle			8	ns	
Crosslink random timeout			1.0	ms	
AC coupling capacitor		75	200	nF	

Table 3-9: PCIE differential Tx output parameter values

Parameter	Symbol	Min	Max	Units	Comments
Unit Interval	UI	399.88 199.94	400.12 200.06	ps	2.5GT/s 5GT/s
Rx eye time opening		0.4		UI	2.5GT/s
Maximum time delta between median and deviation from median			0.3	UI	2.5GT/s
Differential Rx peak-to-peak voltage, common Refclk Rx architecture	$V_{Rx-DIFF-PP-CC}$	0.175 0.120	1.2 1.2	V	2.5GT/s 5GT/s
Differential Rx peak-to-peak voltage, data clocked Rx architecture	$V_{Rx-DIFF-PP-DC}$	0.175 0.100	1.2 1.2	V	2.5GT/s 5GT/s
Maximum Rx inherent total timing error, common Refclk Rx architecture			0.4	UI	5GT/s
Maximum Rx inherent total timing error, data clocked Rx architecture			0.34	UI	5GT/s
Maximum Rx inherent deterministic timing error, common Refclk Rx architecture			0.30	UI	5GT/s
Maximum Rx inherent deterministic timing error, data clocked Rx architecture			0.24	UI	5GT/s
Minimum pulse width at Rx		0.6		UI	
AC peak common mode input voltage			150	mV	
Differential return loss		15		dB	
Common mode return loss		0	3.6	dB	
DC differential input impedance		80	120	ohm	
DC input impedance		40	60	ohm	
Powered down DC input impedance		200		kohm	
Electrical idle detect threshold		65	175	mV	
Unexpected electrical idle enter detect threshold integration time			10	ms	
Total skew			20	ns	

Table 3-10: PCIE differential Rx input parameter values

3.6.3 USB

The USB host interface is powered from VDD33.

Parameter	Symbol	Min	Max	Units	Comments
Output differential peak to peak voltage swing		0.8	1.2	V	
Output differential peak to peak voltage swing, low power		0.4	1.2	V	
Output AC common mode voltage active, peak-peak			100	mV	
Output emphasis		3	4	dB	
Output DC differential output impedance		72	120	ohm	
Output DC common mode impedance		18	30	ohm	
Output frequency slew rate			10	ms/s	
Output jitter, deterministic, delta-delta			0.205	UI	

Table 3-11: USB 3.0 driver specification

Parameter	Symbol	Min	Max	Units	Comments
Input differential sensitivity		30		mV	
Input Low Frequency Signaling detect threshold		100	300	mV	
Input DC differential impedance		72	120	ohm	
Input DC common mode impedance		18	30	ohm	
Voltage change allowed during receiver detection			600	mV	

Table 3-12: USB 3.0 receiver specification

Parameter	Symbol	Min	Max	Units	Comments
Baud rate			480	Mbps	Typical value
Baud rate tolerance		-500	500	ppm	
Data output high		360	440	mV	
Data output low		-10	10	mV	
Data output rise time		500		ns	

Table 3-13: USB 2.0 specification

3.6.4 Digital input/output pad (VDDIO, VIO_SD)

The digital I/O pads are of type none inverting three-state driver/receiver. It includes an input buffer and an output buffer with enable/disable control inputs. It also includes a hold-function. When an I/O is neither driven by the internal nor by an external circuitry, the hold function maintains the latest state of the I/O.

Parameter	Symbol	Min	Typ	Max	Units	Comments
Input low voltage	V_{IL}	-0.4		0.3*V_{IO}	V	
Input high voltage	V_{IH}	0.7*V_{IO}		V_{IO}+0.4	V	
Input leakage current	I_{IL}	-5		5	µA	
Input hysteresis	V_{HYS}	100			mV	
Output low voltage	V_{OL}	-		0.4	V	I_{out}<10mA
Output high voltage	V_{OH}	V_{IO}-0.4			V	I_{out}<10mA
Input pin capacitance	C_{IP}		2.5		pF	

Table 3-14: I/O pin DC characteristics.

3.6.5 PCIe pad ratings (VDDIO)

3.3V operation, PCIE_WAKEn, PCIE_CLKREQ)

Parameter	Symbol	Min	Typ	Max	Units	Comments
Input low voltage	V_{IL}	-0.4		0.8	V	
Input high voltage	V_{IH}	2.0		3.63	V	
Input hysteresis	V_{HYS}	150			mV	
Output low voltage	V_{OL}	-		0.4	V	

Table 3-15: PCIe pin DC characteristics.

4 PIN CONFIGURATIONS

4.1 Pin Configuration SPB228 Module

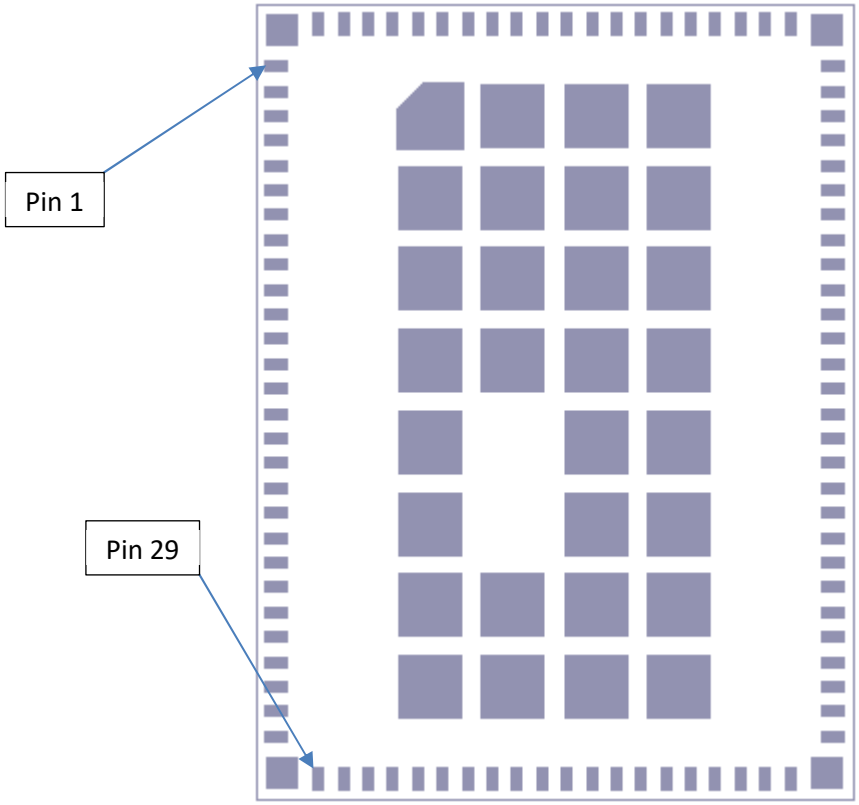

Figure 4-1: Package pin out, top view

4.2 Pin assignments

Pin	Function	Type	Description
1	NC	-	No Connection
2	NC	-	No Connection
3	NC	-	No Connection
4	VDD33	S	Connect to +3.3V supply
5	VDD33	S	Connect to +3.3V supply
6	GND	S	Ground
7	NC	-	No Connection
8	CONFIG_HOST0	I	Configuration Interface Input 0
9	CONFIG_HOST1	I	Configuration Interface Input 1
10	CONFIG_HOST2	I	Configuration Interface Input 2
11	GPIO17	I/O	General purpose IO UART_LTE_TX Output JTAG_TDO

Pin	Function	Type	Description
12	GPIO16	I/O	General purpose IO UART_LTE_RX Input JTAG TDI
13	CONFIG_HOST3	I	Configuration Interface Input 3
14	NC	-	No Connection
15	GPIO1	I/O	General Purpose IO
16	NC	-	No Connection
17	GND	S	Ground
18	GPIO25	I/O	General Purpose IO
19	NC	-	No Connection
20	GND	S	Ground
21	GPIO26	I/O	General Purpose IO
22	GPIO27	I/O	General Purpose IO
23	GND	S	Ground
24	ATEST0	-	Do not connect
25	NC	-	No Connection
26	GND	S	Ground
27	SLP_CLK_IN	I	Sleep Clock Input
28	GPIO13	I/O	General Purpose IO
29	PCIE_WAKEn	I/O	PCIE Wakeup (active low)
30	PCIE_CLKREQn	I/O	PCIE Clock Request (active low)
31	PCIE_PERSTn	I/O	PCIE Reset Input (active low)
32	GND	S	Ground
33	PCIE_RCLK_N		PCIE Clock neg
34	PCIE_RCLK_P		PCIE Clock pos
35	GND	S	Ground
36	PCIE_TX_N/USB3_TX_N	O	PCIE Tx neg USB3 Tx neg
37	PCIE_TX_P/USB3_TX_P	O	PCIE Tx pos USB3 Tx pos
38	GND	S	Ground
39	PCIE_RX_N/USB3_RX_N	I	PCIE Rx neg USB3 Rx neg
40	PCIE_RX_P/USB3_RX_P	I	PCIE Rx pos USB3 Rx pos
41	GND	S	Ground

Pin	Function	Type	Description
42	GPIO0	I/O	General Purpose IO XOSC_EN/Clock Request Output (active high)
43	NC	-	No Connection
44	VIO_SD	S	Connect to IO supply of SDIO
45	PDn	I	Power Down Input (active low)
46	GPIO14	I/O	General Purpose IO JTAG TCK
47	SD_DAT3	I/O	SDIO Data 3
48	SD_DAT2	I/O	SDIO Data 2
49	SD_DAT1	I/O	SDIO Data 1
50	SD_DAT0	I/O	SDIO Data 0
51	SD_CMD	I/O	SDIO Command
52	SD_CLK	I	SDIO Clock Input
53	GPIO12	I/O	General Purpose IO
54	UART_CTSn	I/O	General Purpose IO UART CTS Input (active low)
55	UART_TXD	I/O	General Purpose IO UART Tx Data Output
56	UART_RXD	I/O	General Purpose IO UART Rx Data Input
57	UART_RTSn	I/O	General Purpose IO UART RTS Output (active low)
58	PCM_SYNC	I/O	PCM Sync
59	PCM_IN	I/O	PCM Data Input
60	PCM_OUT	I/O	PCM Data Output
61	PCM_CLK	I/O	PCM Clock
62	GND	S	Ground
63	W_DISABLEn	I/O	PCIE Wireless Disable Input (active low)
64	GPIO2	I/O	General Purpose IO LED Output WLAN
65	GPIO3	I/O	General Purpose IO LED Output BT
66	GPIO15	I/O	General purpose IO JTAG TMS
67	NC	-	No connection
68	GND	S	Ground
69	USB_DM	I/O	USB2 Data neg
70	USB_DP	I/O	USB2 Data pos
71	GND	S	Ground

Pin	Function	Type	Description
72	VDD33	S	Connect to +3.3V supply
73	VDDIO	S	Connect to IO supply, could be different from SDIO supply
74	GND	S	Ground
75	GND	S	Ground
76	GND	S	Ground
77	GND	S	Ground
78	GND	S	Ground
79	GND	S	Ground
80	GND	S	Ground
81	GND	S	Ground
82	GND	S	Ground
83	GND	S	Ground
84	GND	S	Ground
85	GND	S	Ground
86	GND	S	Ground
87	GND	S	Ground
88	GND	S	Ground
89	GND	S	Ground
90	GND	S	Ground
91	GND	S	Ground
92	GND	S	Ground
93	GND	S	Ground
94	GND	S	Ground
95	GND	S	Ground
96	GND	S	Ground

Table 4-1: Pin Description for SPB228 Module

All pads in the middle of the module should be connected to GND as well as the four corner pads.

5 APPLICATION INFORMATION

5.1 Power Supply

SPB228 should be powered by a single supply voltage on VDD33 of 3.3V. It generates all required digital and analog supply voltages with the built- in DC-DC converter. Ramp time applying VDD to SPB228 shall be less than 5ms (<5ms).

5.1.1 Supply

The main power is connected to VDD33. The IO voltage for the SDIO host interface should be supplied to VIO_SD. All other digital IOs should be supplied from VDDIO.
Maximum peak current is approximately 1A.

5.1.2 DC-DC Voltages

The SPB228 has two built in DC-DC converters to generate the required DC voltages. There is no need for external components.

5.2 Clock Signals

The SPB228 requires no external clock signals. It has an internal high frequency oscillator with a high precision 40 MHz crystal and a low power oscillator to generate the required clock signals.

The SPB228 has a built in 32kHz sleep clock. Connect an external 32 kHz clock to SLP_CLK_IN to achieve minimum current consumption. If no external sleep clock reference is used leave the SLP_CLK_IN pin unconnected.

5.3 Enable pin

The Power Down pin (PDn) is internally connected to VDD33 via a 100k pull-up.

Pulling PDn pin low, sets SPB228 in Standby mode. This turns OFF most parts of the circuit and minimizes the current consumption. All I/O interface pins are set to predefined states (high, low or high-z) when in Standby mode.

To end Standby mode set PDn high and reload firmware.

5.4 Power save

Power save is an energy saving mode where SPB228 is only listening at regular intervals for the beacons transmitted from an access point and is set in sleep mode in between. During this sleep mode, firmware is kept in RAM but all not needed functions are turned off. Since the receive time is very short compared to the listening interval the average current consumption is reduced significantly.
The timing of the listening interval is based on the low power oscillator clock generated internally.

5.5 Interfaces

5.5.1 Host interface

The SPB228 supports four host interfaces:

- SDIO
- PCIe
- USB 2.0/3.0
- UART (BT only)

The interfaces are configured on the CONFIG_HOSTx signals during boot. The pins have internal pull-ups and do not require any external circuitry to be set as “1”. Connect 100 kohm to GND to set the signal to “0”.

CONFIG_HOST[2:0]	WLAN Interface	Bluetooth BLE Interface	Driver Name
001	SDIO	SDIO	linux-sdio-driver-228
010	PCIe	USB 2.0	linux-pcie-usb-driver-228
011	PCIe	UART	linux-pcie-uart-driver-228
101	USB 2.0	USB 2.0	linux-usb-driver-228
110	USB 3.0/2.0	USB 3.0/2.0	linux-usb-driver-228
111	USB 3.0	USB 3.0	linux-usb-driver-228

Table 5-1: Host Interface Configuration

5.5.2 PCM Interface

PCM interface is used for BT audio and can operate in master or slave mode. The interface supports the following:

- 8, 13, 14, 15 or 16-bit samples
- 4 slots per frame with up to 16-bits per slot
- Long or short frame sync

5.5.3 Host Wake up

Wake up command via the SDIO interface. This is the normal wake up and is implemented in the FW.

There are options to use defined pin 18 GPIO for Host Wake-up or opposite for SPB228 Wake-Up involving both WLAN, BT.

5.5.4 RF interface

The two RF outputs are MHF4 receptacle micro connectors. They are compatible with MM4829-2702 (HSC series) from muRata, 20449-001E from IPEX, C87P101-C0001-H from Speedtech or W.FL2-R-SMT from Hirose.

5.6 General application information

5.6.1 Design directions

Avoid routing any signals directly under the module. Especially, do not have any signal via holes under the module as there is a risk that they will be shorted to the module.

Make sure that the power supply can handle the large peak currents of up to 1A. The module will do a self-calibration a short time after the start-up when the current could be up to 1A.

All RF is internal to the module and in the two MHF4 connectors. So, there is no need for impedance matched traces for the RF lines.

The PCIE/USB3 lines (TX_N, TX_P, RX_N, RX_P, RCLK_N and RCLK_P) have the following restrictions:

- The length of the balanced signal should be matched
- The single ended impedance should be 60 Ω +/- 15%
- The differential impedance should be 100 Ω +/- 20%
- Use only GND in the layers adjacent to the signal layer, i.e. no other traces crossing

5.6.2 Antenna Connectors

The antenna connector is of type MHF4. The following connectors are compatible:

Vendor	Type	Plug part number
Ipex	MHF4	20448-001R-08
muRata	HSC	MHXP32
Hirose	W.FL2	W.FL2-2LP-xxx
Speedtech	RF4	C87P112

5.6.3 Soldering

The SPB228 is a LGA 1216 module. The recommended solder profile is pictured in Figure 5-1.

Before assembly it is recommended to bake SPB228 for 8 days at 40°C and RH<5% in Tape&Reel or for 16 hours at 125°C with no packaging.

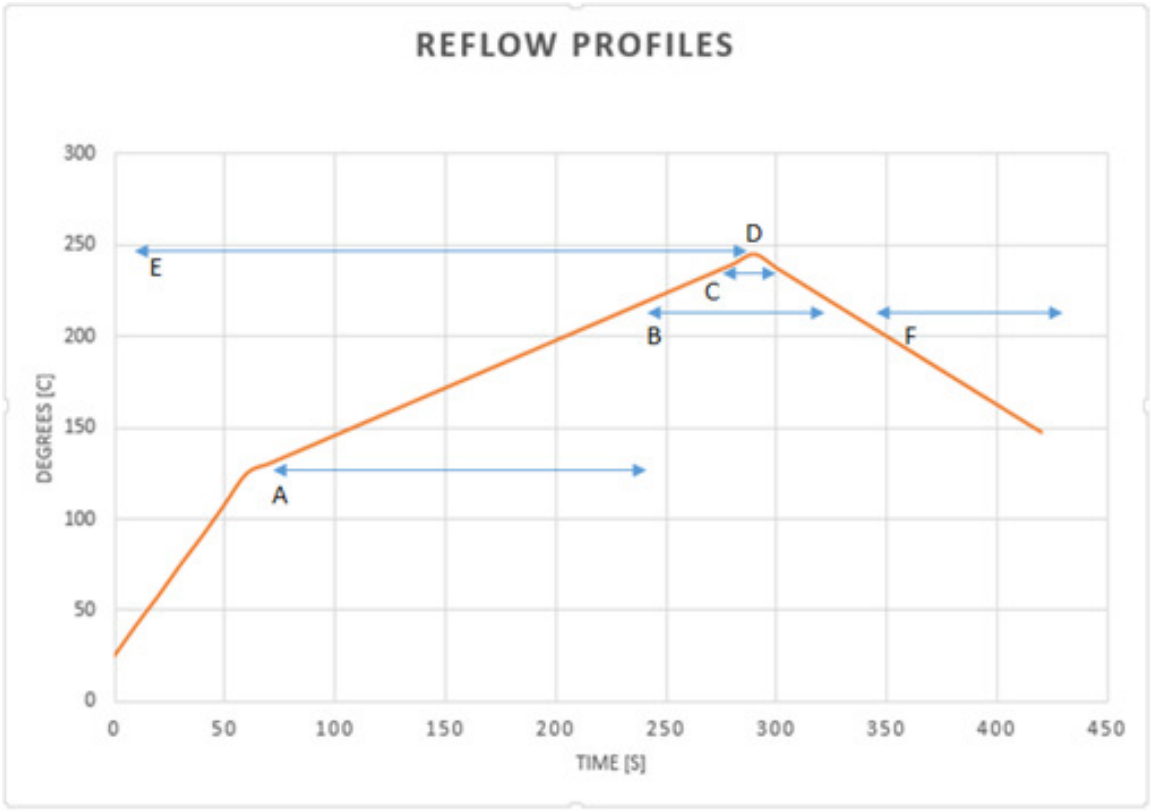

Figure 5-1: Reflow Temperature Profile

Item	Description	Temp	Time
A	Preheat ramp up rate	125-217°C	150-210s
B	Time at >217° C	>217°C	60-90s
C	Wetting time	>235°C	10-30s
D	Peak temperature	245°C	
E	Time from room to peak	25-245°C	240-360s
F	Ramp down temperature	<1°C/s	

Table 5-2: Solder Profile Specification

5.6.4 Environmental statement

The SPB228 is designed and manufactured to comply with the RoHS and Green Directives Package Specifications

5.7 Mechanical SPB228 PCB Module

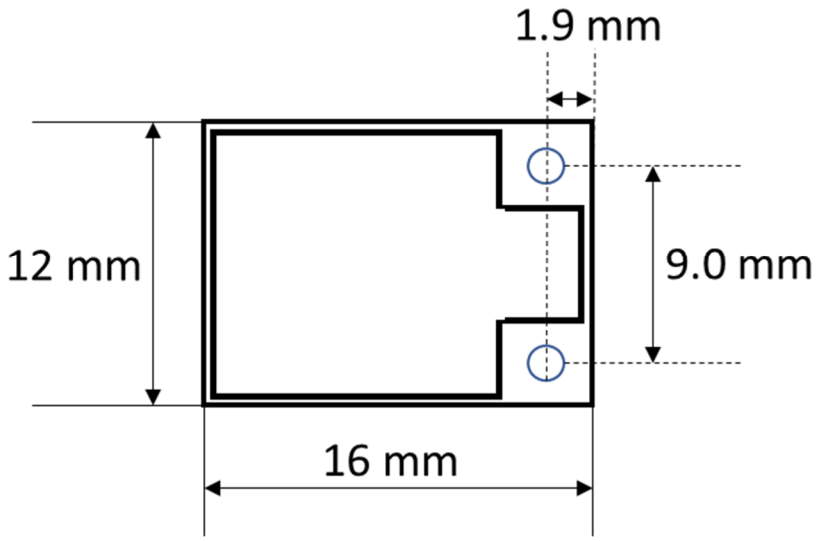

Figure 5-2: Top view

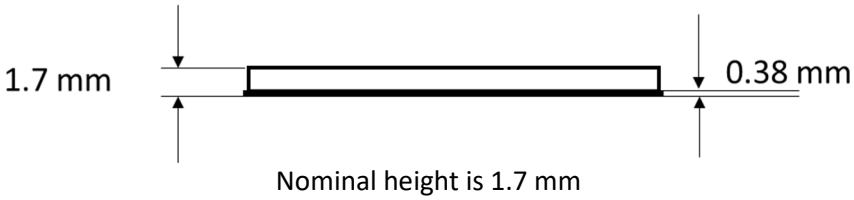

Figure 5-3: Side view

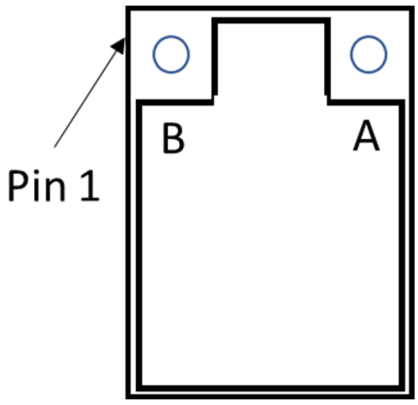

Figure 5-4: Pin 1 position

5.8 Marking SPB228

The module is imprinted with product number and lot number.

5.9 Mounting Information

5.9.1 Pad sizes for SPB228

The following picture describe the solder mask openings on the module. Top view.
Use either 1:1 pad openings or 0.05 mm bigger pads on the mother board. i.e. use either 0.3 x 0.425 mm or 0.35 x 0.475 mm for the 96 signal pads. The solder paste openings for the 1.3 x 1.3 mm GND pads in the middle of the module might need to be reduced with as much as 50% and preferably each GND pad should be divided into four smaller rectangles in the paste stencil. Any open through via hole in the pad should then be placed outside the paste opening.

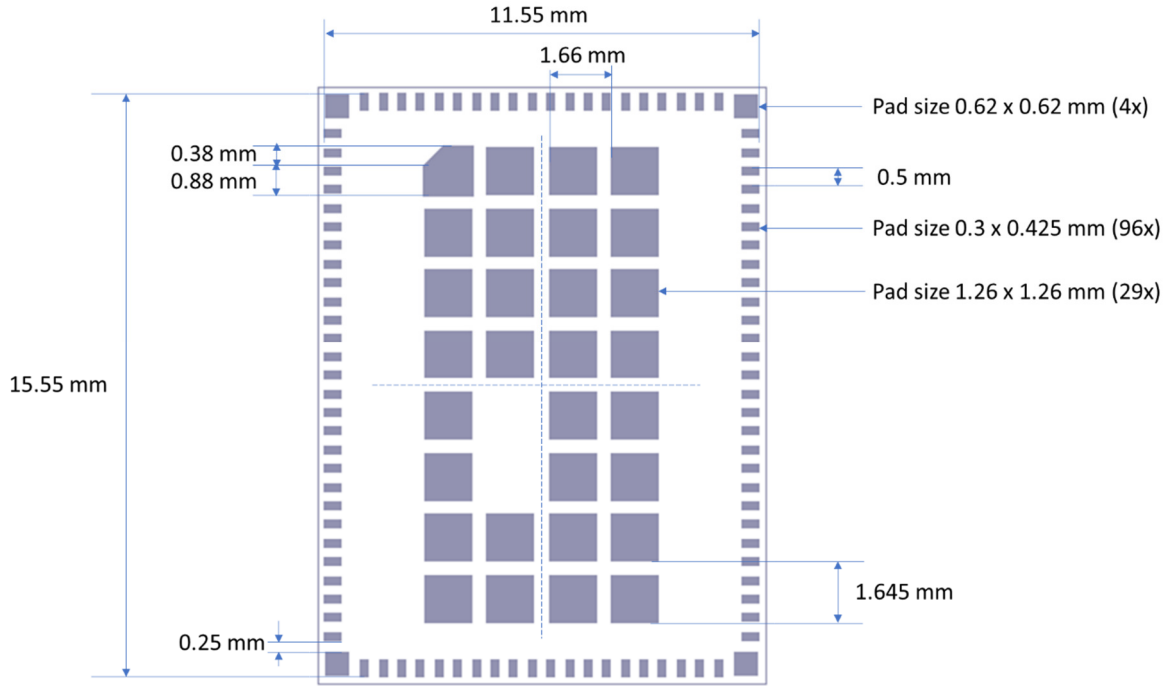

Figure 5-5: SPB228-D land pattern

6 STANDARDS COMPLIANCE

6.1 IEEE/IETF

Standard	Revision	Description
802.11	802.11™ –R2003	WLAN MAC& PHY
802.11a	IEEE 802.11a-1999	OFDM waveform at 5.8 GHz
802.11ac	IEEE 802.11ac	Amendment to IEEE 802.11, wider channels and higher order modulation
802.11b	802.11™ –R2003	High Rate DSSS (5,5/11 Mbit/s)
802.11d	802.11™ –R2003	Operation in different regulatory domains
802.11e	-2005	Quality of Service
802.11g	-2003	Extended rate PHY (ERP-PBCC, DSS-OFDM)
802.11i	-2004	Security enhancements
802.11n	-2009	WLAN MAC&PHY Amendment 5
802.11r	-2008	Amendment 2: Fast Basic Service Set (BSS) Transition
802.11h	1997 edition	Bridge tunneling
802.11w	-2009	Protected Management Frames (PMF)
RFC1042	Inherent	Frame encapsulation

Table6-1: applicable IEEE standards

6.2 Wi-Fi

Specification	Description	Revision
Wi-Fi 802.11b with WPA system inter operability test plan for IEEE 802.11b devices	802.11b devices with WPA	2.1
WiFi 802.11g with WPA system inter operability test plan	802.11g devices with WPA	2.0
WMM (including WMM Power Save)		Ver 1.2
WPS (Wireless Protected Setup)		

Table 6-2: Applicable Wi-Fi standards

6.3 Regulatory

Country	Approval authority	Regulatory	Frequency band
USA	FCC	FCC ID: XO2-SPB228D	2.412 GHz -2.472 GHz 5.180 GHz – 5.825 GHz
Canada	IC	IC: 8713A-SPB228D	2.412 GHz -2.472 GHz 5.180 GHz – 5.825 GHz
Europe		ETSI/EN	2.412 GHz -2.472 GHz 5.180 GHz – 5.700 GHz

Table 6-3: Regulatory standards

6.3.1 FCC (United States of America)

This equipment complies with Part 15 of the FCC rules and regulations.
To fulfill FCC Certification requirements, an OEM manufacturer must comply with the following regulations:

1. The modular transmitter must be labeled with its own FCC ID number, and, if the FCC ID is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following:

Example of label required for OEM product containing SPB228 module

Contains FCC ID: XO2-SPB228D
The enclosed device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions: (i) this device may not cause harmful interference and (ii) this device must accept any interference received, including interference that may cause undesired operation.

2. Only antennas approved may be used with the SPB228 module. The SPB228 module may be integrated with custom design antennas which OEM installer must authorize following the FCC 15.21 requirements.

SPB228 is approved with the following antennas:

Brand	Model	Type	Gain @ 2.4GHz	Gain @ 5GHz	Cable Length
Maglayers	MSA-4008-25GC1-A2	PIFA	2.98 dBi	5.16 dBi	150±5 mm
Bondale	G-RA0K10090176-1436B	Dipole	1.9 dBi	3.6 dBi	120 mm
San Jose	UEN-201	Dipole	2.4 dBi	4.4 dBi	120 mm
Unictron	H2B1PC1A1C175L	PCB	1.6 dBi	4.8 dBi	100±5 mm
LSR	001-0012	Dipole	2 dBi	2 dBi	100 mm
Laird	MAF94051	Dipole	2.4 dBi	3.4 dBi	100 mm
Taoglas	GW.59.3153	Dipole	2.86 dBi	4.74 dBi	100 mm
Chang Hong	DA-2458-02-SMR	Dipole	2.85 dBi	2.17 dBi	100 mm
Unictron	H2B1PD1A1C385L	PCB	2.8 dBi	4.2 dBi	100 mm
Molex	2042811100	PCB	2.562 dBi	3.094 dBi	100 mm
Molex	1461531100	PCB	1.829 dBi	2.485 dBi	100 mm

IMPORTANT: This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation (FCC 15.19).

The internal / external antenna(s) used for this mobile transmitter must provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

This device is approved as a mobile device with respect to RF exposure compliance, and may only be marketed to OEM installers. Use in portable exposure conditions (FCC 2.1093) requires separate equipment authorization.

IMPORTANT: Modifications not expressly approved by this company could void the user's authority to operate this equipment (FCC section 15.21).

IMPORTANT: The finished product is required to comply with all applicable FCC equipment authorizations regulations, requirements and equipment functions not associated with the transmitter module portion. Compliance for unintentional radiators (Part 15 Subpart B “Unintentional Radiators”), such as digital devices, computer peripherals, radio receivers, etc. must be demonstrated.

6.3.2 ISED (Canada)

The device complies with Industry Canada’s license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

Cet appareil est conforme aux normes d’exemption de licence RSS d’Industry Canada. Son fonctionnement est soumis aux deux conditions suivantes:

(1) cet appareil ne doit pas causer d’interférence, et
(2) cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement.

The host product shall be properly labelled to identify the modules within the host product.

The ISED Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labelled to display the ISED Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:

Contains IC: 8713A-SPB228D

Le produit hôte devra être correctement étiqueté, de façon à permettre l'identification des modules qui s'y trouvent.

L'étiquette d'homologation d'un module ISED Canada devra être posée sur le produit hôte à un endroit bien en vue, en tout temps. En l'absence d'étiquette, le produit hôte doit porter une étiquette sur laquelle figure le numéro d'homologation du module ISED Canada, précédé du mot « contient », ou d'une formulation similaire allant dans le même sens et qui va comme suit:

Contient IC: 8713A-SPB228D

6.3.3 ETSI (Europe)

The SPB228 module has been certified for use in European union countries according to ETSI EN 300 328 (Electromagnetic compatibility and Radio spectrum matters for equipment operating in the 2,4 GHz ISM band using spread spectrum modulation techniques) and EN 301 893 (5 GHz RLAN). These standards are harmonized within the European Union and covering essential requirements under article 3 of the Radio Equipment Directive (RED).

If the SPB228 module is incorporated into a product, the manufacturer must ensure compliance of the final end-user product to the European harmonized EMC and low voltage/safety standards. A declaration of conformity must be issued for the product including compliance references to these standards. Underlying the declaration of conformity a technical construction file (TCF), including all relevant test reports and technical documentation, must be issued and kept on file as described in the Radio Equipment Directive.

Furthermore, the manufacturer must maintain a copy of the SPB228 module documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation

requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a complete re-test must be made in order to comply with all relevant standards as basis for CE-marking. A submission to notified body must be used only if deviations from standards have been found or if non-harmonized standards have been used.

7 SALES

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Local sales offices and distributors see **www.hd-wireless.com**

8 TRADEMARKS

- Wi-Fi is a trademark of Wi-Fi Alliance
- Bluetooth is a trademark of Bluetooth SIG