Product Change Notification

Title:	Phoenix PE4H Power Rail Sequencing	
Our reference:	CN-0010-01	
Date:	2nd July 2014	
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Product(s) affected:	Active Silicon products affected by this change:	
	 Phoenix Camera Link Frame Grabber (D48-PE4H): AS-PHX-D48CL-PE4H Phoenix Camera Link Frame Grabber (D64-PE4H): AS-PHX-D64CL-PE4H 	
Description of change:	C22 is changed from 1nF to 3.3nF. R63 is fitted as 330R.	
Affect that change has on operation:	This change improves the ability of the board to lock to the PCI Express signals at start-up; without this modification some boards may appear non-functional in some motherboards after a system boot.	
How to identify original and changed product:	Check the Build Issue and MOD REC on either the product label, or the box label. On older boards the two digit issue is shown following "Iss" or "Issue", and the Mod Rec letter(s) in a separate Mod Rec box. On recent boards the two are combined following "ISS", e.g. "04A" for issue 04, with Mod Rec A applied. See examples on the following page.	
	The following products have the above change applied:	
	AS-PHX-D48CL-PE4H	
	Issue 01 with MOD REC B applied.	
	Issue 02 with MOD REC A applied.	
	Issue 03 with MOD REC A applied.	
	Issue 04 with MOD REC A applied, and higher.	
	AS-PHX-D64CL-PE4H	
	Issue 01 with MOD REC B applied.	
	Issue 02 with MOD REC A applied.	
	Issue 03 with MOD REC A applied.	
	Issue 04 and higher.	
	Note that other MOD RECs may also be marked on the product label but it is only the MOD REC shown above that defines this modification.	
Date that changed product will be shipped:	With immediate effect.	
Notes:	Further information about the need to implement this modification can be found in the <i>Application Note 0.9</i> for the <i>GL9714 PCI Express PIPE x4 PHY</i> dated 9th June 2014 from IC manufacturer Genesys Logic, Inc. See section 11, titled <i>Power Sequence</i> .	
	In detail, changing C22 slows the ramp up rate of the 1.8V internal power rail relative to the 1.2V and 2.5V rails, and R63 is fitted to hold the GL9714 PCIe PHY in reset before the FPGA is configured.	



