Active Silicon   *SNAPPER-PCI-16*
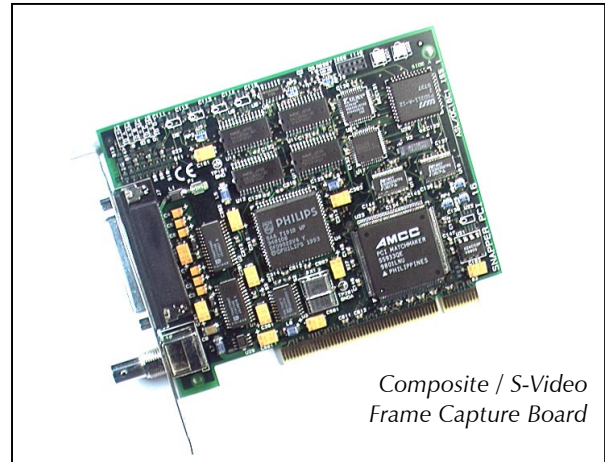
COMPOSITE • S-VIDEO • MONOCHROME VIDEO DIGITIZER

- High quality 16 bit YUV 4:2:2 digital video.
- Decoding of PAL, NTSC and SECAM colour encoded signals in composite or S-Video formats.
- Square pixel sampling for CCIR and EIA standards.
- 1 Mbyte frame store on.
- Hardware Region of Interest (ROI) and sub-sampling.
- Supports asynchronous reset cameras.
- External trigger input available.
- Three software selectable video input sources.
- PCI bus interface supporting 132 Mbytes/sec burst transfers. Support for master and slave operation.
- On-board Data Mapper for hardware pixel mappings.
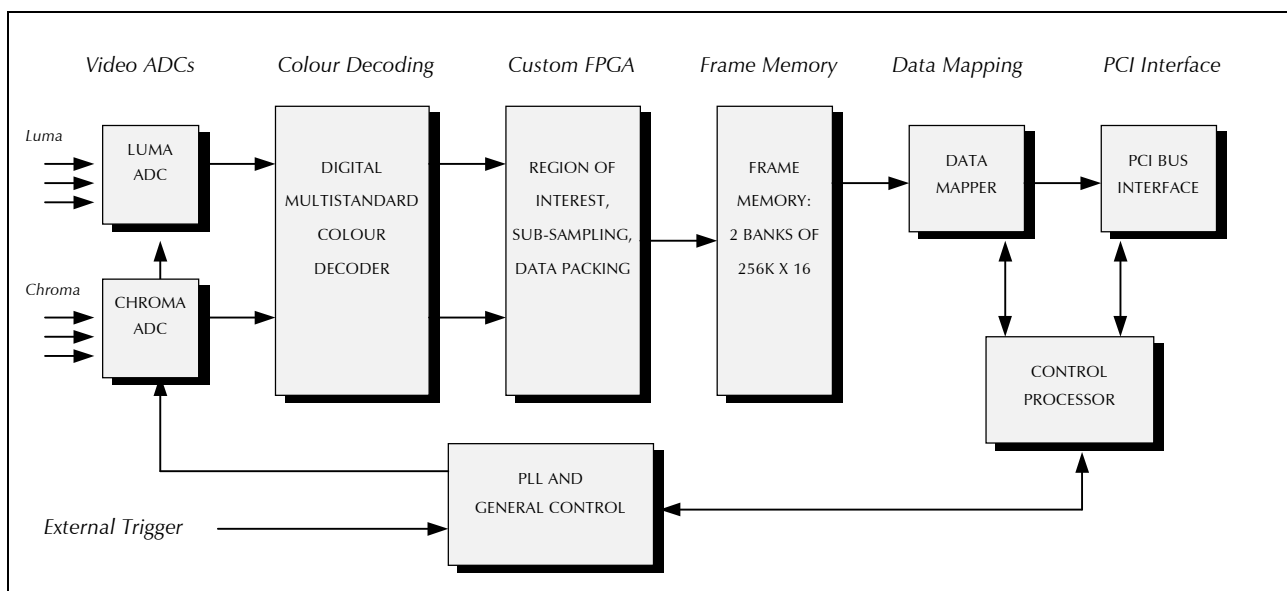- Software Development Kit (SDK) for rapid integration.

Composite / S-Video Frame Capture Board

OVERVIEW

Snapper-PCI-16 is a compact module for the acquisition of standard CCIR or EIA (RS-170) video (i.e. both European and American standards). Full resolution colour (PAL/NTSC/SECAM) or monochrome images are digitized in real-time and stored in on-board frame memory. The Philips 4:2:2 digital video square pixel sampling chipset is used to implement digitization and colour decoding. A custom FPGA (field programmable gate array) then performs optional filtering, sub-sampling and region of interest generation for optimum image quality and readout speed. The frame buffer consists of two banks, each 256K by 16 bits deep, totalling 1 Mbyte. Colour data is stored as YUV 4:2:2 (16 bits per pixel) and monochrome data as efficient byte packed 16 bit words. The frame memory architecture allows de-interlacing on readout. **Snapper-PCI-16** also contains a PCI interface capable of bursting data at 66Mbytes per second for grayscale or colour images.

The Software Developer's Kit (SDK), available as a separate item, allows rapid system development and integration. It provides comprehensive example applications and optimised libraries, and is available for a variety of operating systems including Windows 3.1x/95/98/NT, MacOS 7/8, MS-DOS, Solaris 2, LynxOS and VxWorks. As well as functions that control the hardware, the libraries include general purpose functions for the manipulation and display of images. A separate datasheet describes the SDK in detail.

Snapper-PCI-16 Block Diagram

| Video ADCs | Colour Decoding | Custom FPGA | Frame Memory | Data Mapping | PCI Interface |

Luma — LUMA ADC → DIGITAL MULTISTANDARD COLOUR DECODER → REGION OF INTEREST, SUB-SAMPLING, DATA PACKING → FRAME MEMORY: 2 BANKS OF 256K X 16 → DATA MAPPER → PCI BUS INTERFACE

Chroma — CHROMA ADC

CONTROL PROCESSOR

External Trigger → PLL AND GENERAL CONTROL

SPECIFICATION

Video Input: The video input consists of three luminance channels and three chrominance channels. Each of these are 75 Ohm terminated. The luminance and chrominance channels each connect to a three to one multiplexer before feeding into the ADCs. The selection of any one of these three video sources is under software control. This input architecture allows up to three S-Video sources; three composite sources or three monochrome sources to be multiplexed into the module.

Sampling: CCIR video frequencies (European) are sampled at 14.75MHz and EIA video frequencies (USA and Japan) at 12.27MHz. This results in square pixel sampling for both standards. The video standard and whether the signal is colour or monochrome can be auto-sensed. Standard S-Video, composite and monochrome is digitized in real-time.

Digital Video: The luminance video signal is digitized to 8 bits with black level at 16 and peak white at 235. The chrominance signal is digitized and decoded to U and V digital components. The U and V component's range is 44 to 212 with 128 as zero for 75% colour bars. Both luminance and chrominance digitization have Automatic Gain Control (AGC). These quantization levels conform to CCIR Recommendation 601-2.

Data Format: The format for digital colour data is standard YUV 4:2:2 - thus consecutive words are read as YU, YV, YU etc, with the luminance (Y) component as the lower byte of the 16 bit word. Grayscale data is packed as 16 bit words consisting of two 8 bit pixels, with the first pixel appearing as the lower byte of the word. It is also possible to map grayscale data from 8 bits to 7 bits in hardware (using a right shift operation). This can be useful when displaying the image to a paletted display, when it may be necessary to reserve colours for window borders and text etc.

Colour Decoder: The colour decoder is a digital decoder which supports PAL, NTSC and SECAM. The decoder auto-senses the colour standard and decodes the signal appropriately.

Resolution: CCIR video images are digitized to a resolution of 768 x 576 and EIA (RS-170) video images to 640 x 480. These resolutions represent the full active (picture) area of the video signal.

Region of Interest: A region of interest (ROI) for acquisition and readout is software programmable. The horizontal start and length are controllable to a resolution of 8 pixels and the vertical start and length are controllable to a resolution of 2 lines. (The vertical start position must be less than 254 lines down the field.) This programmable ROI allows a faster frame readout rate if, for example, the module is used on the ISA bus, which is limited to about 2 Mbytes per second data transfer.

Sub-sampling: Sub-sampling can be performed in hardware and is software programmable. Sub-sampling can be by two or by four:
x2: Every 2nd pixel in the horizontal direction and only the first field of each frame.
x4: Every 4th pixel in the horizontal direction and every second line of the first field of each frame.
A horizontal digital filter implemented in the FPGA can also be software enabled to reduce aliasing effects.

Frame Store: The video frame store consists of 1 Mbyte of RAM configured as FIFO memory. The memory is arranged as two banks of 256K by 16 - one bank for each video field. This allows the captured video image to be de-interlaced on readout by switching banks on a line by line basis. This de-interlacing method is actually hidden to the user in the software library, but is described here to provide a thorough understanding.

Readout Time: The access time for the video data is 12ns and the cycle time is 60ns. This results in a maximum readout rate of 33 Mbytes/second.

Trigger: A separate TTL input is provided for synchronisation to external events - for example to synchronise to a strobed flash gun. The polarity of the trigger input is software programmable. Asynchronous reset cameras are fully supported in this mode.

Controls: Control of brightness, contrast and colour is performed in software. The hardware uses an AGC for both brightness and colour level to achieve optimum image quality.

Interrupts: An interrupt signal is available and can be configured via software to interrupt on "acquisition complete" when running from external trigger or normal next frame capture. Polled operation is also supported.

PCI BUS INTERFACE SPECIFICATION (INCLUDING DATA MAPPER)

Interface: PCI (Peripheral Component Interconnect) Bus to PCI Local Bus Specification Revision 2.1 using 5V signalling environment.

Data Mapper: 8 bit grayscale or 24 bit RGB can be mapped to 32 bit RGBX, XBGR, BGRX, XRGB or to 16 bit RGB as RGB16 or RGB15. (16 bit output formats such as RGB16 are automatically packed to 32 bits prior to PCI bus transfer).

Data Rates: Bus master DMA supports 132 Mbytes/sec data transfer rate. The PCI data is generated by the Data Mapper reading from the Frame Buffer memory. For YUV data 2 pixels are transferred on alternate PCI clocks, whereas for grayscale data, 4 pixels are transferred on alternate PCI clocks.

Address Range and Automatically mapped to I/O space. Board requires 64 bytes of address space.
Interrupts: Interrupts automatically selected by host operating system.

PHYSICAL AND ENVIRONMENTAL DETAILS

Dimensions:	107mm by 84mm.
Approximate weight:	65g.
Maximum component height:	4.7mm.
Mounting pillar height:	10mm.
Snapper connectors:	Two 50 way, 0.1" pitch connectors, each arranged as two rows of 25.
Power consumption:	+5V @ 0.8 Amp typical (1 Amp maximum).
	+12V @ 60mA typical (80mA maximum).
	(Option at time of manufacture for only using a 5V supply).
Storage Temperature:	-15°C to +70°C.
Operating Temperature:	0°C to +55°C.
Relative Humidity:	10% to 90% non-condensing (operating and storage).
EMC Approvals:	$C\epsilon$ mark for compliance with EN 55022:1994 (class B) and EN 50082-1:1992 in accordance with EU directive 89/336/EEC.
	FCC Class A.

Full mechanical drawings are available on request.

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
SNP-PCI-16	**Snapper-PCI-16** composite/S-Video frame capture module.
CBL-25D-SNP	Standard cable assembly which consists of one S-Video input, three composite/monochrome inputs, a trigger input and an analogue sync input (which is not applicable to **Snapper-PCI-16**). Other custom cables can be made to order. Please contact Active Silicon for more information.
-	Software Developer's Kit. For a full list of all supported operating systems, support contracts and other options, please refer to the SDK datasheet, or contact Active Silicon directly. Currently supported operating systems include Windows NT, Windows 95, Windows 98, Windows 3.1x, MS-DOS, Solaris 2, VxWorks, LynxOS and MacOS.

ORDERING NOTES

- For users requiring a single composite/monochrome input, the BNC connector can be used which then only requires a simple co-ax connection.
- Please contact Active Silicon for latest information on other Snappers, Bus Interface Boards, and supported operating systems.

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Additional Technical Information for Snapper-16

Connector Pinout

A 25 way D type socket connects signals into the module.

Pin Number	Snapper-16
1	GND
2	**Luma 2**
3	**Chroma 1**
4	Chroma 3
5	N/C
6	N/C
7	N/C
8	+12V out
9	N/C
10	N/C
11	N/C
12	N/C
13	GND
14	Luma 1
15	*Luma 3*
16	Chroma 2
17	N/C
18	N/C
19	N/C
20	N/C
21	Trigger
22	N/C
23	N/C
24	N/C
25	N/C

NOTES:

1. The signal names in ***bold italics*** are available on the standard cable, (Part number CBL-25D-SNP).
2. Signals labelled as *Sig+* and *Sig-* are the two halves of the RS-422 signals and must be connected to twisted pair cabling.
3. When using the TTL level trigger, connect the input to *TRIGGER+*.

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